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A Unified Phase-Shift Modulation for Optimized Synchronization of Parallel Resonant Inverters in High Frequency Power System

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Abstract: This project present advanced configuration for Symmetric multilevel voltage source inverter is proposed. The Authority of the proposed inverter versus the conventional Cascaded H-bridge inverter and the most recently introduced ones, is verified with provided comparisons. The proposed Inverter is able to generate the desired voltage levels using a Lower number of circuit devices including power semi-conductor Switches and related gate driver circuits of switches. This modular structure uses reduced number of Devices, including its power semiconductor switches and gate Driver circuits of switches. As a result, the total cost is considerably reduced and the control scheme gets Simpler. Moreover, reduced amount of on-state switches in the Suggested configuration decreases voltage drops even, the suggested multilevel Inverter has the lowest amount of power losses. Finally simulation and experimental results are compared with each other and the provided comparison shows that the obtained results are in good Agreements.

1. INTRODUCTION

The high frequency alternating current (HFAC) power distribution system (PDS) has already become a preferred alternative to the traditional dc distribution system in computer and telecom , electric vehicle , and renewable energy micro grid. The merits of HFAC can be generally summarized by: 1) flexible conversion of different voltage grades; 2) effective electrical isolation using compact high frequency transformers; 3) significant saving in component count and size; 4) improvement in the system dynamic response; 5) reduction or elimination of acoustic noise; and 6) more safety with increasing frequency. A typical structure diagram of HFAC PDS as shown in Fig. 1(a) is formed by the source and the load side. The source side is constructed by a number of front-end inverters in parallel connection to deliver power from the input line to the transmission track, and the load side is constituted by point-of-use converters to absorb the power from the transmission track. High performance resonant inverter serves as the HFAC source side to provide HF output, flexible power expansion capability, and better load performance. However, the control of the resonant inverter is complicated in HFAC circumstance because of the following factors: 1) Input voltage varies over a wide scope; 2) HF power expansion is difficult; 3) soft switching is required to operate in a wide range; 4) output voltage with low total harmonic distortion (THD) is necessary for precise load; and 5) unknown distributed load and multiple load interactions lead to more dynamic and nonlinear characteristics. Therefore, great efforts from topology, modulation, and control strategy have been done to solve these issues in HFAC power source.

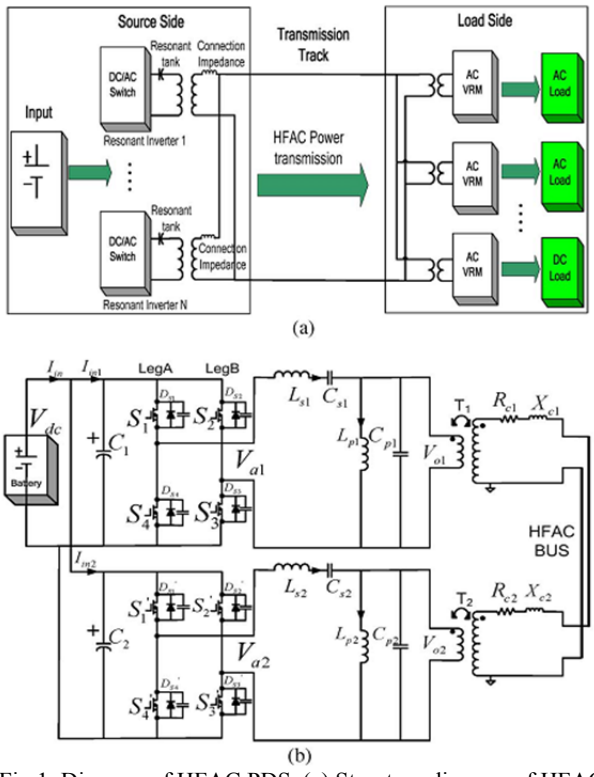


Fig.1. Diagram of HFAC PDS. (a) Structure diagram of HFAC PDS. b) Single-stage resonant inverter with full bridge PSM in parallel connection

From the view of topology, a variety of high frequency resonant inverters are presented High frequency ac–ac can also be found in matrix power converters. Most of them can be divided into the switching network and resonant tank, in which the switching network converts the dc voltage to a quasi-square waveform and the resonant tank designed for the harmonic filter also provides zero voltage switching (ZVS) conditions. The single-stage

phase-shift modulation (PSM) resonant inverter constructed by full bridge and inductor capacitor-inductor-capacitor (LCLC) resonant tank is the best candidate of HF power source because of outstanding comprehensive abilities. The full bridge provides the large power grade with less switch stress. It is easy to implement ZVS at fixed frequency in PSM. The resonant tank formed by four energy storage components provides the sinusoidal output with less THD and more flexible ZVS configuration. Thus, the rational HF power source as shown in Fig. 1(b) is a parallel system constructed by a single-stage resonant inverter. The connection impedance (Zc = Rc + jXc) is deliberately placed to prevent the circulating current, and it also is non negligible because of the connection cable.

Another very important approach to solve the aforementioned high frequency issues is the appropriate strategy of modulation and control. The advanced magnitude controller is proposed to regulate the resonant converter. However, most of them are complicated and costly. A frequency-based controller titled by one cycle robust controller was easy to be implemented by discrete devices and can effectively resist the perturbations from input line, load, and components, but the exclusive magnitude control is far from enough for load sharing in parallel system. Because of the prominent discrepancy of phase angle, the unavoidable circulation current and the unwanted power losses are severe in parallel system. The current sharing control (CSC) algorithm accomplishes high frequency load sharing using average magnitude and phasor transformer. However, the phasor transformer-based CSC is complicated, and the average magnitude-based CSC needs an unperturbed phase angle. A symmetrical PSM is proposed to maintain the phase angle unperturbed in magnitude modulation. However, it only provides a rough current sharing because it fails to consider output discrepancy from component tolerance in connection impedance and series–parallel resonant tank (Ls, Lp, Cs, Cp). In order to perfectly accomplish current sharing in parallel system, independent phase control is indispensable to operate with magnitude control together. An independent small-signal based phase controller is proposed for the two-stage resonant inverter but it uses separated power circuit to regulate the magnitude and phase. If the regulations of phase and magnitude can be integrated together by a unified modulation, optimized synchronization and advanced CSC can be achieved in the parallel single-stage resonant inverter.

Power factor (PF) is the cosine of the angular difference between voltage and current. It is P.F = cos (Vs^Is). It can vary ϕ calculated as PF = cos between zero and one depending on the type of load. If the supply voltage and current are in-phase with each other, then the power factor of the circuit ($\cos\phi$) is unity. The power electronic switching devices introduce distortion into the system. As a result, the power factor gets lowered. The diode bridge rectifier with capacitive filter is used as the fundamental block of many power electronics converters. Due to its non-linear nature, non-sinusoidal current is drawn from the utility and harmonics are injected into the utility lines. The injected current has lower order of harmonics and causes voltage distortion and poor power factor at input AC mains. This causes slow varying ripples at DC output load resulting in lower efficiency and larger size of AC and DC filter. These converters are required to operate with high switching frequencies due to demand for small filter size and high power density. High-switching frequency operation results in higher switching losses, increased electromagnetic interference (EMI), noise and reduced converter efficiency. To overcome these drawbacks, the switches of buck-boost converter are operated with zero voltage and zero current switching. High-switching frequency with SS provides low switching stress and losses, high-power density, less volume and lowered ratings for the components, high reliability and efficiency. To improve the efficiency, a large number of soft switching technique including resonant circuits have been proposed. But these converters increase the number of switches and stages in power conversion circuit thus complicating the sequence of switching operation, excessive voltage and current stresses, and also narrower line and load ranges.

This paper describes a single stage AC-DC converter with high power factor. For high power application power handling capacity is increased so full bridge resonant converter is adopted which is combined with two Buck-boost type PFC circuits. Two active power switches act as a PFC circuits Therefore, power handing capacity increased. A high power factor at the input line is achieved by operating the PFCs at discontinuous conduction mode. The output voltage is regulated by controlling the ON/OFF time of switches present in buck-boost converter. The higher order harmonics are eliminated by using low pass filter, which reduce the size of filter and increases the power factor. Here soft switching can be obtained by using a new partial resonant converter. The higher order harmonics are eliminated by using low pass filter, which reduce the size of filter and increases the power factor. Here soft switching can be obtained by using a full bridge resonant converter. The proposed system has the advantage of less components and less switching losses.

2. LITERATURE REVIEW

2.1 AC/DC CONVERTER TOPOLOGIES FOR THE SPACE STATION

A new class of AC/DC converter topologies (Type-1 converters) is described, suitable for use in an advanced single-phase sine-wave voltage, high-frequency power distribution system, of the type that was proposed for a 20 kHz Space Station primary electrical power distribution system. The converter comprises a transformer, a resonant network, a current controller, a diode rectifier, and an output filter. The input AC voltage source is converted into a sinusoidal current source using the resonant network. The output of this current source is rectified by the diode rectifier and is controlled by the current controller. The controlled rectified current is then filtered by the output filter to obtain a constant voltage across the load. Three distinct converter topologies, Type-1A, Type-1B, and Type 1-C, are described, and their performance characteristics are presented. All three types have a close-to-unity rated power factor (greater than 0.98),

low total harmonic distortion in input current (less than 5%), and high conversion efficiency (greater than 96%)

2.2 A POWER FACTOR CORRECTED AC-AC INVERTER TOPOLOGY USING A UNIFIED CONTROLLER FOR HIGH FREQUENCY POWER DISTRIBUTION ARCHITECTURE

This paper presents an AC-AC inverter for high frequency power distribution architecture. The inverter includes a high frequency resonant inverter and a buck-boost power factor correction stage. A unified controller controls both the resonant inverter and power factor correction stages. Unlike other single stage power factor corrected inverter topologies, the proposed inverter system has reduced DC bus voltage stress for the universal input line voltage. The proposed inverter is found attractive in low power applications

2.3 HIGH FREQUENCY AC VS. DC DISTRIBUTION SYSTEM FOR NEXT GENERATION HYBRID ELECTRIC VEHICLE

The paper proposes and then demonstrates the viability of high frequency AC (HFAC) for propulsion power distribution system in the next generation advanced electric/hybrid vehicle. In justifying this viability, the HFAC system has been studied thoroughly and compared with the traditional DC distribution system with regard to cost, weight, performance and other capabilities after performing component sizing calculation of both the systems. The superior features of HFAC system are highlighted, and its possible drawbacks an mentioned. The DC, resonant link DC and HFAC (single-phase and polyphase) distribution systems have been discussed. The single phase HFAC system is shows to be superior to the others. A preliminary modelling, control strategy development and computer simulation study validate the feasibility of HFAC for propulsion power distribution system

2.4 A LOW FREQUENCY AC TO HIGH FREQUENCY AC INVERTER WITH BUILD-IN POWER FACTOR CORRECTION AND SOFT-SWITCHING

This paper describes a single stage AC- DC converter with high power factor. The diode- capacitor type of rectifier cause low power factor because of its nonlinearity. PFC serves to smooth out power drawn and regulates the output voltage. High power factor at the input is assured by operating the buck-boost converter at discontinuous conduction mode of operation. With same operation on both cycle and detailed designed circuit parameter, zero- voltage switching on all the active switches of the converter can be retained to achieve good efficiency. This gives soft switching condition which increases the efficiency of the system and reduces the switching power losses. The buck boost converter and the filter circuit are used to re-shape the input current waveform so as to be in phase with input voltage waveform. The design, analysis, simulation and hardware realization of the AC-DC converter with soft switching. This mode begins at when turning off the MOSFETs (M2 and M3), since the load current ir is negative at the switching off time. The diodes (D9 and D12) are forced to free wheel ir. The drain to sources voltage (Vds2 and Vds3) of M2 and M3 are combined to -0.7 v. The voltage across the resonant circuit is equal to dc-link voltage Vdc3 and Vdc4.After some time gating signal are given to MOSFETs (M1& M4) but there are still in off condition. The voltage in the reactive component L1 is equal to the line voltage. The inductor current Ip1 increases linearly from zero. Then M1 is turned on at zero voltage.

Since the circuit operates equally, the operation of the negative half cycle of the line voltage are equal to positive half cycle, except for inductor and power factor correction circuit .Hence the circuit is analyzed for positive half cycle only. The circuit operation divided into seven modes of operation with respect to conducting switches. Each modes are explained below.

2.5 AUTOMATED OPTIMAL DESIGN OF INPUT FILTERS FOR DIRECT AC/AC MATRIX CONVERTERS

This paper presents a novel method to design the input filter for a direct ac/ac matrix converter using genetic algorithms (GA) optimization. The input filter for a matrix converter is a very important and critical part of the conversion structure and careful design is necessary to ensure high input power quality, compactness, and stability. The GA will optimize structure and parameters of the input filter as a function of different factors such as energy storage, weight, and volume. The effectiveness of this design method is demonstrated through a wide range of simulations using Saber and experimental results on a laboratory prototype. The same methodology could also be adapted and applied to any converter configuration such as, for example, traditional voltage source converters

3. SYSTEM STUDY

3.1 EXISTING SYSTEM

The single-stage phase-shift modulation (PSM) resonant inverter constructed by full bridge and inductor capacitor-inductor-capacitor (LCLC) resonant tank is the best candidate of HF power source because of outstanding comprehensive abilities. The full bridge provides the large power grade with less switch stress. It is easy to implement ZVS at fixed frequency in PSM. The resonant tank formed by four energy storage components provides the sinusoidal output with less THD and more flexible ZVS configuration. Thus, the rational HF power source as shown in Fig. 1(b) is a parallel system constructed by a single-stage resonant inverter. The connection impedance (Zc=Rc+jXc) is deliberately placed to prevent the circulating current, and it also is non negligible magnitude and phase. If the regulations of phase and magnitude can be integrated together by a unified modulation, optimized synchronization and advanced CSC can be achieved in the parallel single-stage resonant inverter.

3.2 PROPOSED SYSTEM

3.2.1 AC PHASE ANALYSIS

The ac phase analysis is accomplished to analyze the relations of phase and component parameters. The equivalent schematic of the resonant inverter is simplified to Fig. 2.

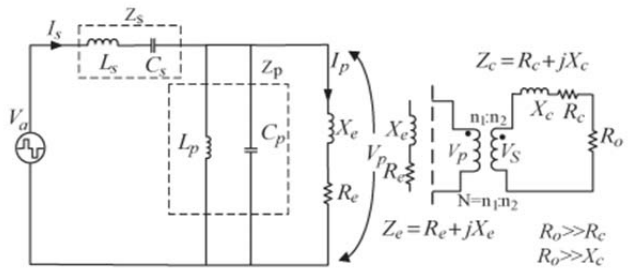


Fig 2. Impedance equivalent circuit of single stage resonant inverter

The input voltage of the resonant tank is an ideal quasi-square wave form Va obtained by full bridge chopping. Xe and Re are the equivalent reactance and resistance from the secondary side, both of which form equivalent impedance Ze. Vp and Vs are the voltages of the primary and secondary sides. N is the turns ratio of the transformer. The connection reactance and resistance (Xc,Rc) are small enough as compared with other circuit parameters. Zs and Zp are the series and parallel impedances of the resonant tank.Ro is the load resistance. The parasite resistances are neglected in impedance equivalent circuit. The Fourier decomposition of Va is

$$v_a(t) = \sum_{n=1,3}^{\infty} \frac{4V_{\text{in}}}{n\pi} \sin\frac{n\delta}{2} \sin\frac{n\pi}{2} \sin(2n\pi f_s t)$$

$$v_{a1}(t) = \frac{4V_{\text{in}}}{\pi} \sin\frac{\delta}{2} \sin(2\pi f_s t) \qquad (1)$$

Where Vin is the input voltage, δ is the pulse width of phase shift magnitude, fs is the switching frequency, and va1is the first harmonic of va. If only the fundamental component is available caused by the ideal filter performance of the LCLC resonant tank, the voltage over the parallel resonant branch or over the equivalent load is Vp1=Va1((Zp1// (Ze1)/(Zs1+Zp1//Ze1)), where Zs1, Zp1,and Ze1 are the fundamental impedances of Zs, Zp, and Ze respectively.

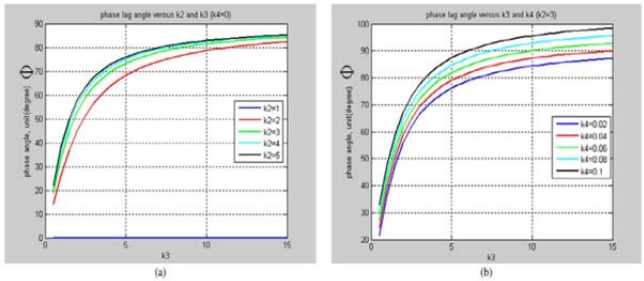


Fig 3.Phase angle curve vs predefined constants a)Phase angle curve vs k2 & k3 with zero k4.b)Phase angle curve vs k2 & k3 with fixed k2.

It is difficult to quantitatively evaluate the relation of phase angle to circuit parameters. Guo and Jain introduced a predefined constant to help with the characteristics analysis of the resonant inverter; however, output phase angle sensitivity with respect to the resonant parameter has not been conducted by them.

4. SYSTEM DEVELOPMENT

4.1 PSM EVOLUTION OF HFAC RESONANT INVERTER

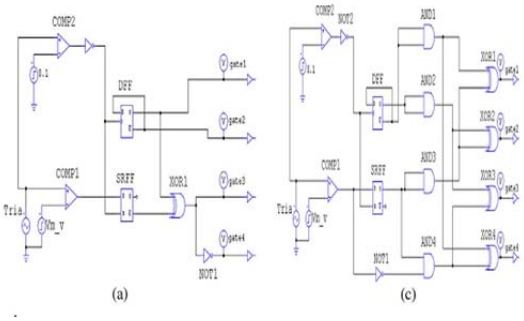
Based on two existing PSM methods (the traditional PSM and the symmetrical PSM), a novel PSM is proposed for the single-stage resonant inverter in parallel connection. A) Analysis of Traditional PSM and Symmetrical PSM The traditional PSM as shown in Fig. 4(a) is made up of two comparators, two D flip-flops, and a few logic gates. Fig. 4(b) demonstrates the typical waveforms of the traditional PSM. The H-bridge contains leading (LEG A) and lagging (LEG B) bridges from each half bridge. The carrier signal is Vc, and the modulation signal is Vm. The full bridge output is Va, and the fundamental portion of Va is Va1 α is the phase-shift angle between leading and lagging bridges. Because of the geometry relationship as α+δ=π, α can be derived by the modulation signal (Vm) as α = (Vpp−Vm/Vpp) π, in which Vpp is the peak voltage of the carrier signal. The traditional PSM generates the varying phase-shift angle α and controls the output magnitude of the resonant inverter via the comparison of the sawtooth carrier Vc and the modulation signal Vm. As shown in Fig. 4(b), the gate signal of the lagging phase is to flip polarity at a fixed point of Vc, while the gate signal of the leading phase is to flip polarity at a controllable point determined by Vm. Therefore, an extra item emerges in output phase angle caused by magnitude modulation. The extra phase angle decided byVmis equal to α/2. Consequently, the magnitude vo(t) and phase ∠vo(t) of output voltage vo(t) in the traditional PSM are described by

$$\|v_o(t)\| = \left\|\frac{Z_s}{Z_s+Z_p}\right\| \frac{4}{\pi} v_{\text{in}} \sin\left(\frac{\pi-\alpha}{2}\right) \left\|\frac{R_o}{R_o+Z_c}\right\|$$

$$\alpha = \frac{(V_{pp}-V_m)}{V_{pp}}\pi$$

$$\angle v_o(t) = \frac{\alpha}{2} + \phi = \frac{(V_{pp}-V_m)}{2V_{pp}}\pi + \angle Z_s + \angle Z_p + \angle Z_c.$$

The output phase in the traditional PSM not only depends on the component parameters as mention earlier but also depends on the magnitude modulation (Vm). Therefore, the traditional PSM fails to get rid of the modulation coupling of magnitude and phase. For instance, if two parallel inverters generate different magnitude modulation signals (Vm and V*m) to balance the magnitude output, traditional modulation leads to undesirable phase difference in inverter outputs to deteriorate load sharing.



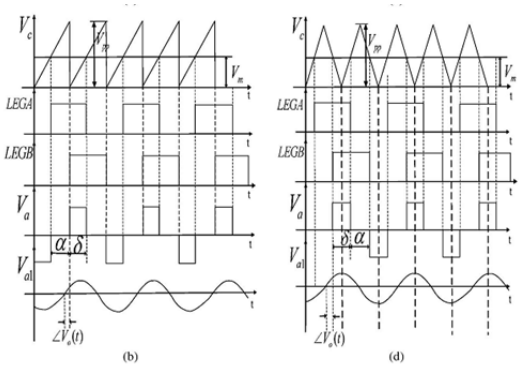


Fig.4. Structures of traditional and symmetrical PSMs.(a) Traditional PSM structure.(b)Operation waveforms of traditional PSM.(c) Sym metrical PSM structure.(d)Operation waveforms of symmetrical PSM

A symmetrical PSM as shown in Fig. 4(c) was proposed to remove the Vm item in ∠vo(t). The typical waveforms in Fig. 4(d) demonstrate the critical operations. A controllable pulse width modulation (PWM) is symmetrically generated by the comparisons of the triangle carrier Vc and modulation signal Vm. The rising edge matching of Vc and Vm triggers the polarity inversion of the leading bridge (LEG A), while the falling edge matching of Vc and Vm triggers the polarity inversion of the lagging bridge (LEG B). The logic operations of gate signals are

$$gate1 = XOR\left\{Q(RS), \bar{Q}(D)\right\}$$

$$gate4 = XOR\left\{AND\left\{Q(RS), NOT(PWM)\right\}, \bar{Q}(D)\right\}$$

The varying Vm simultaneously moves the gate signals of the leading and lagging bridges at opposite direction, so the midpoint of Va is located in a fixed position with respect to Vc As a result, ∠vo(t) keeps fixed in the course of magnitude regulation, and the Vm item in ∠vo(t) is removed by symmetrical PSM.

$$\|v_o(t)\| = \left\|\frac{Z_s}{Z_s + Z_p}\right\| \frac{4}{\pi} v_{\text{in}} \sin\left(\frac{\pi - \alpha}{2}\right) \left\|\frac{R_o}{R_o + Z_c}\right\|$$

$$\alpha = \frac{(V_{pp} - V_m)}{V_{pp}} \pi$$

$$\angle v_o(t) = \phi = \angle Z_s + \angle Z_p + \angle Z_c.$$

Vo(t) and ∠Vo(t) in the symmetrical PSM are shows below. As shown in fig 5, the ∠Vo(t) only depends on component parameters in the symmetrical PSM. If two parallel inverters generate different magnitude modulation signals (Vm and Vm) to balance the magnitude output, the symmetrical PSM provides near-identical phase angle in two inverter outputs. However, the discrepancy of ∠Vo(t) is unavoidable in the symmetrical PSM caused by the component tolerance of parallel resonant inverters.

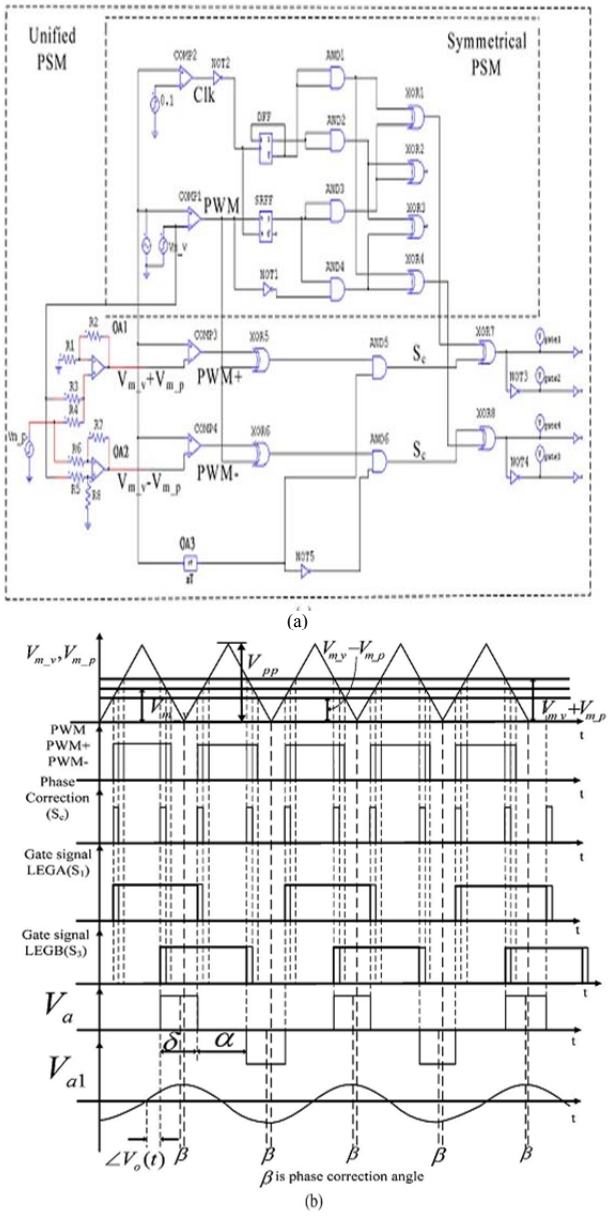


Fig. 5. Unified PSM. (a) Structure. (b) Operation waveforms

4.2 PROPOSED UNIFIED PSM

The traditional PSM has a phase perturbation from magnitude modulation, and the symmetrical PSM fails to eliminate phase discrepancy from component tolerance. A novel modulation circuit called as unified PSM is proposed to solve these issues so that output discrepancy is minimized and optimized synchronization is achieved.

First, 10% parameter tolerance with Gaussian distribution is supposed to exist in parallel inverters. Moreover, the parallel resonant inverters employ the same carrier with the same frequency and phase. The unified PSM as shown in Fig.5(a) contains three operational amplifiers (summing, difference, and differentiator), two comparators, and more logic gates than the symmetrical PSM. From the viewpoint of functionality, the circuit structure is divided into three parts. The first one is to generate the symmetrical PSM using triangular carrier Vc and magnitude modulation signal Vm. The second one is to separate the phase correction from magnitude regulation.

The last one is the directional logic to select an accurate correction pulse.

The typical waveforms as shown in Fig. 5(b) demonstrate the logic fundamentals of the unified PSM. Sc is the phase correction pulse.S1 and S3 are the driver signals of LEG A and LEG B, respectively. The carrier period is the half of the switching period. The dead time and other time losses are ignored as compared with the switching period.

Vm_v is the output of the magnitude controller, which is used to generate the equivalent PWM through the comparison of Vm_v to triangular carrier Vc. A quasi-square waveform generated by the equivalent PWM is symmetrical to Vc because the gate signal in the leading bridge is decided by the rising edge matching of Vc and the gate signal in the lagging bridge is determined by the falling edge matching of Vc. Therefore, the upper part in Fig. 5(a) is the typical circuit of the symmetrical PSM. Furthermore,Vm_pas the output of the phase controller is calculated by operational amplifiers (OA1 and OA2) to retrieve Vm_v+Vm_p and Vm_v−Vm_p. Three PWM signals (PWM, PWM+, & PWM-) are obtained by the comparison of Vc to the modulation signal (Vm_v, Vm_v+Vm_p & Vm_v− Vm_p). Phase correction pulses Scin PWM+/PWM- are subsequently split by two exclusive OR (XOR) gates (XOR5 and XOR6). The obtained Sc comprises four types, i.e., the pulses of the leading/lagging bridge and the pulses of the forward/backward direction, which are discriminated by the selection logic formed by the differentiator and logic gates (OA3, AND5, and AND6). The valid correction pulses are correspondingly superimposed onto the original gate signal via another two XOR gates (XOR7 and XOR8). Because new modulation simultaneously moves the leading and lagging bridges in the same direction, δ and Vo(t) remain unchangeable in the phase regulation. ∠Vo(t) also keeps fixed in the magnitude regulation as the symmetrical PSM does. Therefore, the regulations of magnitude and phase can coexist in the unified PSM. Finally, Vo(t) and ∠Vo(t) in the unified PSM are

$$\|v_o(t)\| = \left\|\frac{Z_s}{Z_s+Z_p}\right\|\frac{4}{\pi}v_{\text{in}}\sin\left(\frac{\pi-\alpha}{2}\right)\left\|\frac{R_o}{R_o+Z_c}\right\|$$

$$\alpha = \frac{(V_{pp}-V_m)}{V_{pp}}\pi$$

$$\angle v_o(t) = \phi+\beta = \angle Z_s+\angle Z_p+\angle Z_c+\beta$$

$$\beta = \frac{V_{m\_p}}{2V_{nn}}\times\pi \qquad (9)$$

Where β decided by Vm_p is the phase regulation angle from the independent phase controller.Phase discrepancy caused by component tolerance and operation conditions is completely compensated by β, so the output synchronization of parallel resonant inverters can be optimized by it. The transient analysis of the unified PSM is conducted by two typical scenarios. One is the transient scenario with varying magnitude and fixed phase. The other one is the transient scenario with varying phase and fixed magnitude. The waveforms of scenario 1 as shown in Fig. 6(a) are divided into three operation stages. Stage I is the steady state with fixed Vm_v and Vm_p, stage II is the transient state with varying Vm_v and fixed Vm_p, and stage III is the new steady state with new fixed Vm_v and original Vm_p.

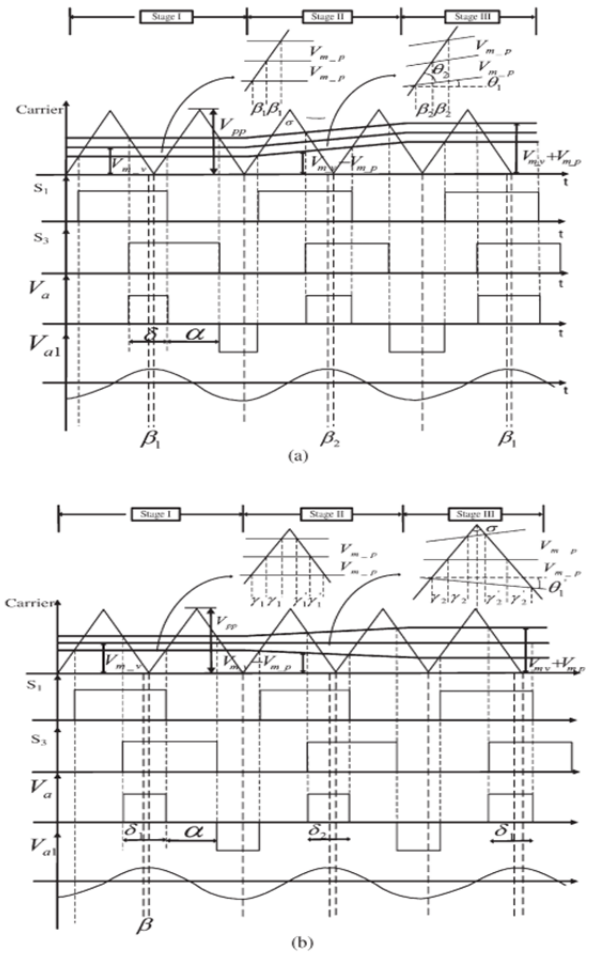


Fig. 6.Waveforms of transient state. (a) Typical waveforms of the varying magnitude modulation with fixed phase modulation. (b) Typical waveforms of the varying phase modulation with fixed magnitude modulation.

The phase regulation angle βshould remain unchangeable in the three stages caused by a fixed Vm_p. However, it changes in stage II due to disturbance from the varying magnitude regulation. The phase regulation angle deviation is

$$\Delta\beta_T = \beta_1-\beta_2$$

$$= \frac{V_{m\_p}}{\tan\theta_2}-\left(\frac{V_{m\_p}}{\tan\theta_2}-\frac{V_{m\_p}}{\tan(90^o-\theta_1)}\right)\cos\theta_1$$

$$\theta_1+\theta_2 = \frac{\pi}{2}-\frac{\sigma}{2} \qquad (10)$$

Where β1 and β2 are the phase regulation angle in stages I and II, respectively, θ1 is the crossing angle of Vm_v to the horizontal line in stage II, θ2 is the crossing angle of Vm_v to carrier Vc in stage II, and σ is the vertical angle of the

carrier. Consequently, the phase regulation deviation ΔβT increases with decreasing θ2.

The waveforms of scenario 2 as shown in Fig. 6(b) are also divided into three operation stages. The difference with scenario 1 is that the transient stage in scenario 2 has a fixed Vm_v and varying Vm_p. Because the phase modulation simultaneously shifts the gate signal of leading and lagging bridges in the same direction, δ should be constant due to a fixed Vm_v. However, the deviation of δ emerges in stage II caused by the disturbance from asymmetrical phase regulation. From the magnified curve of Fig. 6(b), the deviation of δ is derived by

$$\Delta\delta_T = \delta_2 - \delta_1 = \frac{2V_{m\_v} \times \Delta\overline{V}_{m\_p} \times \tan\theta_1'}{V_{pp}}$$

Where δ1 and δ2 are the magnitude widths in stages I and II, respectively. $\Delta\overline{\ }$Vm_p is the Vm_p variation in one carrier period, and θ1 is the crossing angle of Vm_p to the horizontal line in stage II. Therefore, the magnitude regulation deviation ΔδT increases with increasing θ1. It is concluded from the two scenarios that both ΔβT and ΔδT exist in transient state, both of which are determined by the slope of Vm_v and Vm_p. A larger slope of Vm_v and Vm_pleads to larger ΔβT and ΔδT. Furthermore, the modulation ratio of the unified PSM can be defined to help the controller design. At the moment of t0, the magnitude modulation is Vm_v(t0), and the phase modulation is Vm_p(t0). After a moment, the magnitude modulation becomes Vm_v(t1), and the phase modulation becomes Vm_p(t1). The difference between t0 and t1 is ΔVm_v = Vm_v(t1)−Vm_v(t0), ΔVm_p = Vm_p(t1)−Vm_p(t0), Δδ = δ(t1)−δ(t0), and Δβ = β(t1)−β(t0). According to the carrier symmetry, modulation ratio (Km_v, Km_p) can be defined by Km_v = (Δδ/ΔVm_v) = (π/Vpp), Km_p = (Δβ/ΔVm_p) = (π/Vpp). Because Km_v is equal to Km_p, both regulations have the same linear scale weight. Similarly, Dm_v and Dm_p are the cross-ratios between magnitude and phase regulations defined by Dm_v = (Δβ/ΔVm_v), Dm_p = (Δδ/ΔVm_p), both of which have already been discussed by typical transient scenarios. Relations of the modulation ratio to the slope of the modulation signal are plotted in Fig. 7.

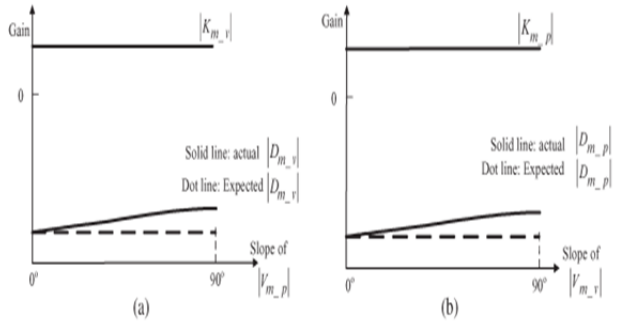


Fig.7 Relations of modulation ratio to the slop of modulation signal Curve of Km-v and Dm-v b)Curve of Km-p and Dm-p

5. System Implementation

5.1 COMPARISONS OF THE THREE PSM

From the aforementioned analysis, the traditional PSM is enough for the dc/dc resonant converter without phase consideration, the symmetrical PSM roughly accomplishes phase synchronization in parallel system, and the unified PSM improves the high frequency synchronization of parallel outputs.The comparisons among the three PSMs are shown in Table I.

TABLE I
COMPARISON OF THREE PSMS

	Phase disturbance from magnitude regulation	Phase control	Possible applications
Traditional PSM	Yes	No	DC/DC resonant converter
Symmetrical PSM	No	No	Parallel resonant inverters without parameter tolerance consideration
Unified PSM	No	Yes	Parallel resonant inverters with parameter tolerance consideration

The unified PSM can independently regulate the phase and magnitude of the output voltage. Output voltage synchronization against component tolerance and operational condition is guaranteed by two independent controllers integrated by the unified PSM. On account of independent control ability, advanced CSC algorithm can be implemented by the unified PSM to accomplish load sharing and circulation current minimization in parallel resonant inverters.

5.2 OPERATION SCOPE OF PROPOSED MODULATION

The operation scope of the proposed modulation is limited by ZVS and THD. The magnitude regulation represented by δ is determined by lower output THD, ZVS in larger operating scope, and less current stress. The phase regulation represented by β is decided by the geometry relationships of β to δ. The foundation of unified modulation is the comparison of modulation and carrier signals, so the modulation signal (Vm_v+ Vm_p,Vm_v−Vm_p, and Vm_v) must be located in the carrier scope, i.e

$$0 \le V_{m\_v} - V_{m\_p} \le V_{m\_v} \le V_{m\_v} + V_{m\_p} \le V_{pp}$$

$$(\delta + \beta \le \pi) \text{ AND } (\delta - \beta \ge 0^o).$$

The output current of the resonant inverter lags behind its voltage, and φ is the phase lag angle between output current and chopped voltage. The ZVS condition in the lagging bridge is φ > (π−δ/2), so the relation of β max to predefined constants can be derived by it

$$\delta > \pi - 2\phi \Rightarrow \delta > \pi - 2\tan^{-1}\left[-k_3\left(\frac{1}{k_2} - 1\right)\right]$$

$$\times \left\{\beta_{\max} \le 2\tan^{-1}\left[-k_3\left(\frac{1}{k_2} - 1\right)\right]\right\} \text{ AND } \{\beta_{\max} \le \delta\}.$$

Furthermore, the output THD of the quasi-square waveform is analyzed at the complete resonance in the resonant tank, i.e., k2=1

$$2\pi f_s L_s = 1/2\pi f_s C_s,\ 2\pi f_s L_p = 1/2\pi f_s C_p$$

$$Z_{sn} = j2\pi f_s \left(1 - \frac{1}{n^2}\right) nL_s$$

$$Z_{pn} = \frac{1}{j\left(2\pi f_s \left(1 - \frac{1}{n^2}\right) nC_p\right)}$$

Where Zsn and Zpn are the nth harmonic impedances of the series and parallel branches (n=1,2,...,∞). The harmonic damping factor (kfn,n=1,2,...,∞) is defined by

$$k_{fn} = \left|\frac{Z_{pn}}{Z_{sn} + Z_{pn}}\right| = \frac{1}{\sqrt{\left(1 - (n - \frac{1}{n})^2 \times k_1\right)^2 + \left(\frac{(n-\frac{1}{n}) \times 2\pi f_s L_s}{R_o}\right)^2}}.$$

Kfn decreases with decreasing Ro, and the minimum kfn lies in the full load condition. When the load is open circuited (k3=∞), the maximum THD is achieved with the largest kfn. Hence, the worst THD is derived by its definition

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} (K_{fn} V_{an})^2}}{V_{a1}} \times 100\% = \frac{\sqrt{\sum_{n=2}^{\infty} \left[\frac{V_{an}}{\left(1-(n-\frac{1}{n})^2 k_1\right)}\right]^2}}{V_{a1}} = \frac{\sqrt{\sum_{n=2}^{\infty} \left[\frac{0.9\sin\left(\frac{n\delta}{2}\right)}{n\left(1-(n-\frac{1}{n})^2 k_1\right)}\right]^2}}{0.9\sin\left(\frac{\delta}{2}\right)}$$

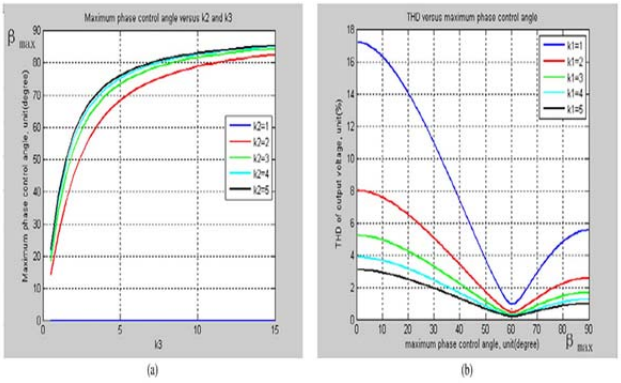


Fig.8 operation scope of βmax a) βmax vs k2& k3 b)worst case THD vs βmax with different k1 & fixed k2=2

Where Va1is the fundamental component of Va and Van is the nth harmonic of Va. According to (13) and (16), the limitations of β are demonstrated in Fig. 8(a), and the curve of output THD versus β max is plotted in Fig. 8(b).

The following conclusions are made from Fig. 8(a): 1) The variation of β maxis located in the range of [0◦,90◦];2) the larger k3 has a larger β max, and k3should be as large as possible to enlarge the operating scope of β, but a larger k3 leads to larger current stresses in the resonant components, so a suitable k3is important to provide an optimized operation scope of β; and 3) the larger k2 has a larger β max because a larger k2 exhibiting a larger inductive impedance achieves ZVS easily.It can be observed from Fig. 8(b) that the larger k1 has the lower THD. The minimum THD is derived near 60 ◦ β, i.e., δ is around 120 ◦ and output THD is less than 2%. Consequently, the operating scope of phase regulation is decided by the circuit parameters and operating condition in the unified PSM.

6. PERFORMANCE EVALUAT I O N

The evaluation of simulation and experiment consists of two parts. One is to testify the feasibility of unified modulation. The other one is to evaluate the synchronization improvement in parallel system.

6.1 FEASIBILITY OF UNIFIED PSM

6.1.1 SIMULATION CIRCUIT:

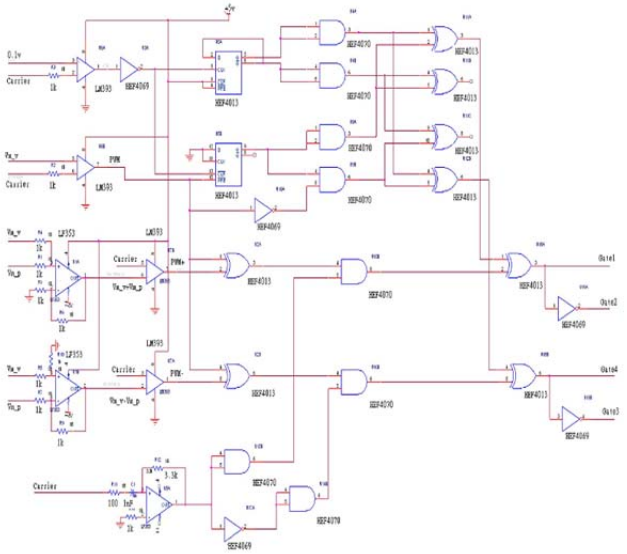


Fig.9 Circuit schematic of unified PSM

To consider the PDS in electrical vehicle with a moderate transmission range, an experimental prototype of the unified PSM was implemented with the operating frequency of 25 kHz. The circuit schematic as shown in Fig. 9 contains more components than the symmetrical PSM, including four XOR gates, three operational amplifiers, two comparators, and three AND gates. Three operational amplifiers with±5-V power supply implement difference, noninverting summing, and differentiator, respectively. LF353 is a dual operational amplifier with a 4-MHz bandwidth operated at dual voltage mode. LM393 is a dual comparator operated at single voltage mode. The logic operation is accomplished by locally oxidized complementary metal-oxide-semiconductor transistor components, including HEF4013 (dual D flip-flop), HEF4070 (Quad 2-input XOR), HEF4081 (Quad 2-input AND gate), and HEF4069 (hex inverters). CMOS logic output is magnified by IR2113 to drive IRF530N.

6.1.2 SIMULATION RESULTS:

The steady and transient states of the unified PSM are simulated by Power SIM (PSIM)to testify the previous analysis. The steady state waveforms.

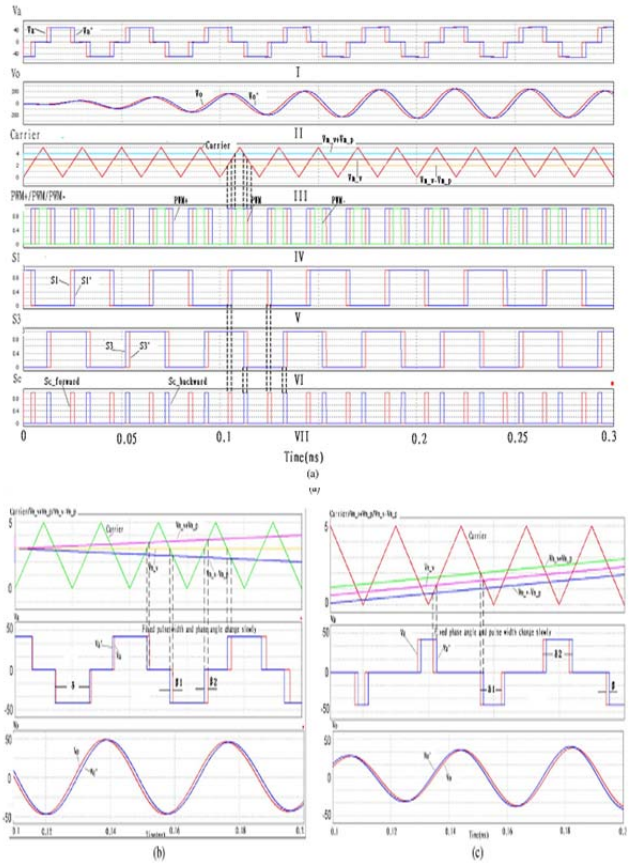


Fig.10 Simulation result of unified PSM. (a) steady state (b)transient state with varied Vm_p(Kp(s) = 0.1,Kv(s) = 0.1 (c)Transient state with varied Vm_v(Kp(s) = 0.1,Kv(s) = 0.1

Fig a I. proves the phase regulation capability. The red and blue lines are the full bridge outputs before and after phase regulation, respectively. a.II further testifies the phase regulation in the corresponding sinusoidal output. a.III shows the modulation signals(Vm_v+Vm_p,Vm_v,Vm_v−Vm_p) and triangular carrier Vc (5VVpp). a. IV shows three PWM signals (PWM, PWM+, and PWM-) obtained by the comparisons of modulation and carrier signals. a.V and a.VI are the gate signals of s the phase compensation pulses (Sc) to be superimposed onto the original the leading and lagging bridges moved in the same direction to obtain a fixed δ.VII.

Simulations in transient state are demonstrated in Fig. 10(b) and (c) with varying Vm_v and Vm_p. Kv(s) and Kp(s) are the controllers of magnitude and phase, both of which use a small proportional constant(Kp(s)=0.1,Kv(s)=0.1)to obtain controller outputs(Vm_v,Vm_p)with the lower slope. With fixed Vm_v and varied Vm_p, δ should be fixed, and β changes slowly. With fixed Vm_p and varied Vm_v, β should be fixed, and δ changes slowly. It is observed from Fig. 9(b) and (c) that both Δδ and Δβ from Dm_v and Dm_p are negligible due to slowly changing Vm_v and Vm_p.

Consequently, simulations in steady or transient state prove that the unified PSM is feasible to integrate the magnitude and phase regulations together.

6.1.3 EXPERIMENT RESULTS:

With a positive Vm_p, the correction signals Sc of the leading and lagging bridges are demonstrated in Fig. 11(a) and (b). In Fig. 11(a), one of four pulses is selected as the forward Sc of the leading bridge, which has the fixed position with respect to the carrier signal. Similarly, the forward Sc of the lagging bridge is shown in Fig. 11(b) with fixed position as well. The correction signals Sc as shown in Fig. 11(c) and (d) have the same selection logic with an egative Vm_p. Therefore, the Sc of different bridges and directions can be obtained by the proposed logic circuit

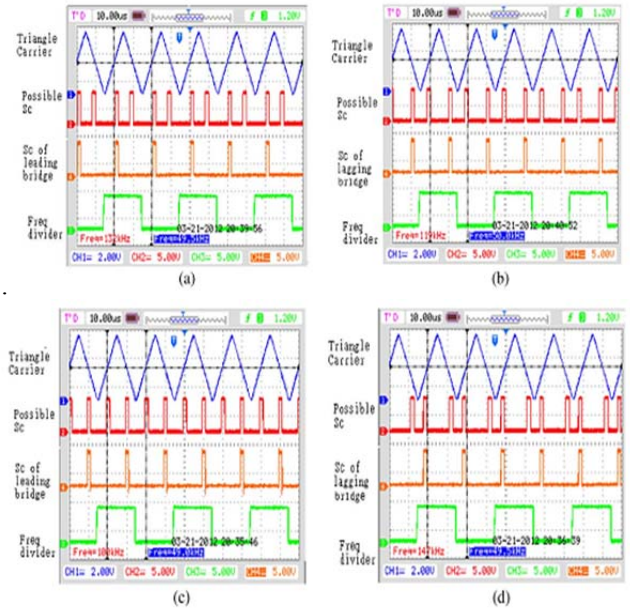


Fig. 11. Experimental waveforms of the phase modulation. (a) Correction pulse of leading bridge(Vm_p=0.8V). (b) Correction pulse of lagging bridge

With a positive Vmp (0.5 V), the full bridge output as shown in Fig. 12(a) has a backward phase regulation.

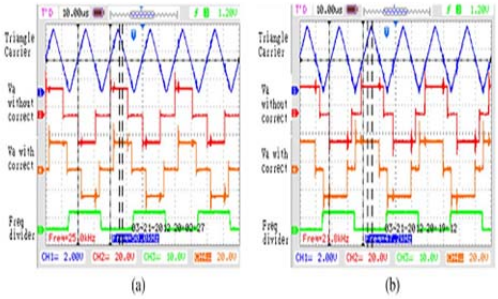
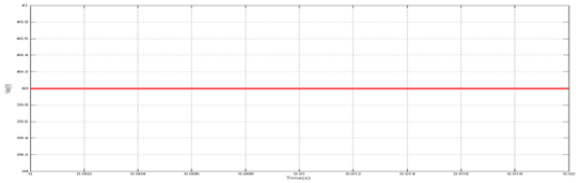


Fig.12. Experimental waveforms of full bridge output. (a) Full bridge output comparison (Vm_p=0.5V,Vm_v=2.5V). (b) Full bridge output comparison (Vm_p=−1V, Vm_v=3V).

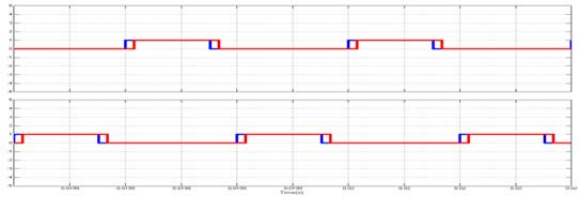
Similarly Fig. 12(b) has a forward phase regulation caused by negative Vm_p(−1V). It is concluded that the unified PSM provides phase regulation with controllable quantity and direction. The pulsewidth control is also testified by Fig. 12 with varied Vm_v (2.5 and 3 V). The full bridge output is a quasi-square waveform with glitches in the intersection point of logic operation. These glitches can be filtered by the snubber circuit and resonant tank afterward.

6.1.4 SIMULATION OUT PUT:

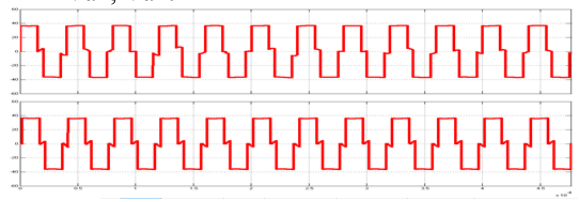
a) Input voltage:



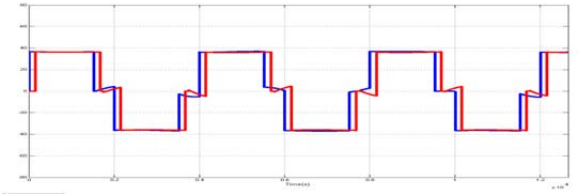
a) Gate Pulse



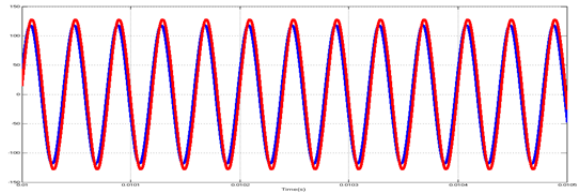
b) Va1, Va2:



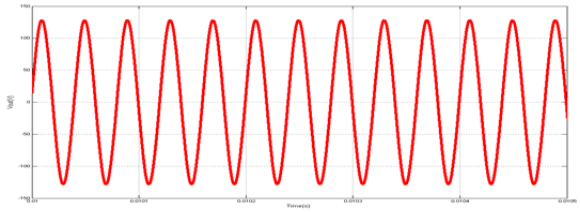
c) VAa1, Va2 in mux:



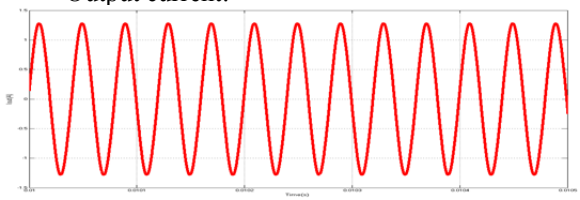
d) V01, V02:



e) Output voltage:



f) Output current:



g) Output power:

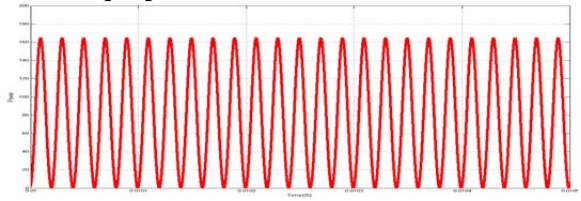
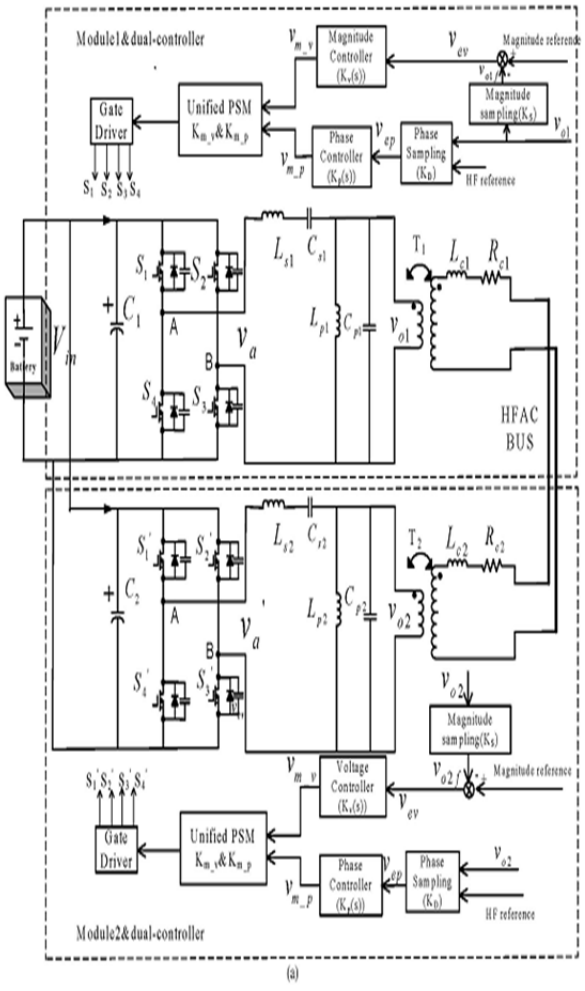


Fig.13 simulation outputs of unified PSM

6.2 UNIFIED PSM IN PARALLEL SYSTEM

Furthermore, a parallel prototype formed by two resonant inverters was established to evaluate the optimized synchronization against component tolerance. The control diagram as shown in Fig. 13(a) is for parallel LCLC resonant inverters with dual-control scheme. The nominal circuit parameters are as follows: 1) input voltage Vin = 20±10%V; 2) rated output peak voltage Vo_pk = 40V; 3) rated output peak current Io_pk = 3−7A (the load scope is 6–13Ω); 4) rated operating frequency fs=25kHz; and 5) resonant tank (Ls1 = 110μH, Lp1 = 53μH, Cs1 = 1.2μF, Cp1 = 0.72μF, Ls2 = 100μH, Lp2 = 50μH, Cs2 = 1.1μF, Cp2 = 0.68μF). The phase error is detected by an analog multiplier (AD633) with detection gain KD. The magnitude error is detected by a low-pass filter with detection gain KS. Moreover, the controllers of magnitude and phase in the dual-control scheme are independent proportional–integral controllers denoted by Kv(s) and Kp(s), respectively. Km_v and Km_p are the modulation ratios of magnitude and phase in the unified PSM. Vev and Vep are the errors of magnitude and phase. Vm_v and Vm_p are the outputs of the magnitude and phase controllers. Because the unified PSM accomplishes magnitude and phase regulations separately, the control schematic as shown in Fig. 13(b) is constituted by independent controllers



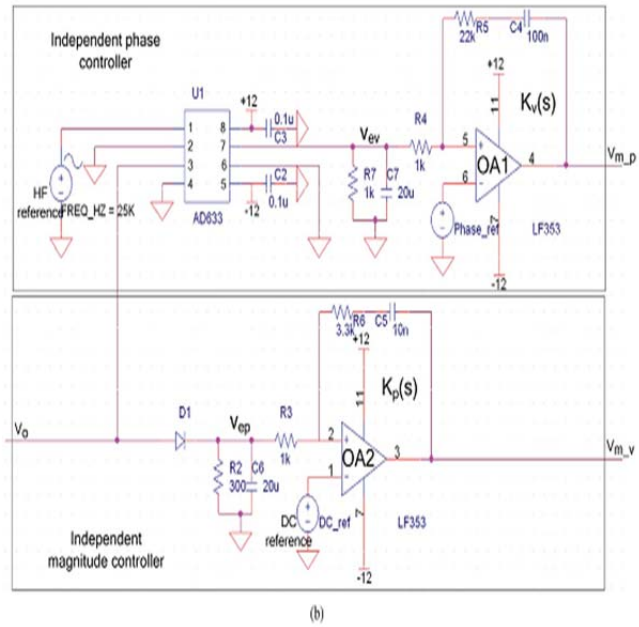


Fig. 14. Control diagram and circuit schematic. (a) Control diagram of dual-control scheme in parallel resonant inverters. (b) Circuit schematic of 2 controllers in single-stage resonant inverter. OA1 forms Kv(s),OA2 forms Kp(s), and the HF reference is a 25-kHz sinusoidal waveform.

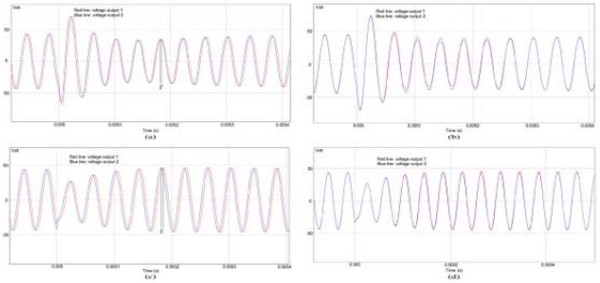


Fig. 15. Dynamic-state simulation with nominal resonant parameters. (a) Load decrease (100%to 50%) using symmetrical PSM with magnitude control. (b) Load decrease (100%to 50%) using unified PSM with dual control. (c) Load increase (50%to 100%) using symmetrical PSM with magnitude control. (d) Load increase (50%to 100%) using unified PSM with dual control

.

6.2.1 SIMULATION RESULTS: The parallel prototype is simulated by PSIM, and the step load response with nominal resonant parameters is accomplished to compare the symmetrical and unified PSM.

A dynamic response is demonstrated in Fig. 14, in which a step load variation occurs at the time of 0.005 s. The step load consists of load increase from 50% to 100% and load decrease from 100% to 50%. It can be observed from Fig. 14(a) and (c) that the voltage output of the parallel inverter has a phase deviation due to the parameter difference of the resonant tank. However, the phase deviation as shown in Fig. 14(b) and (d) is compensated by the phase controller in unified modulation. The simulation results prove that the optimized synchronization is achieved by the proposed scheme, and the optimized synchronization against parameter tolerance is significant to accomplish averaging magnitude based CSC.

6.2.2 EXPERIMENTAL RESULTS:

The experiment is conducted by parallel platform with the different parameter configurations in resonant tank and connection impedance. The steady-state outputs of the parallel prototype are shown in Fig. 15. With the introduction of component tolerance, parallel inverter outputs as shown in Fig. 15(a) and (c) have phase deviation ξ, which fails to be compensated by the exclusive magnitude controller in the symmetrical PSM. It can be found from Fig. 15(b) and (d) that the phase deviation ξ is perfectly compensated forward and backward in the unified PSM. Therefore, the proposed scheme is superior to the symmetrical PSM due to an optimized synchronization in steady stage. Further dynamic results of load variation are conducted by the parallel prototype. The waveforms as shown in Fig. 16(a) and (c) reveal the phase deviations (ξ1, ξ2, and ξ3) in steady and dynamic states, which are prominent in the symmetrical PSM with magnitude control. It is observed from Fig. 16(b) and (d) that the phase difference in dynamic response is almost eliminated by the unified PSM with dual-control scheme. The experimental results agree with the simulation. On account of the uncertainties from the component tolerance, control.

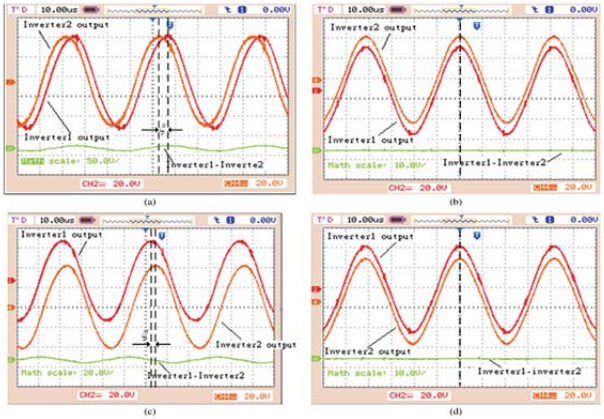


Fig.16. Comparison of steady-state outputs.

(a) Inverter output in symmetrical PSM with magnitude control (Rc1=Rc2= 500mΩ, Lc1=2μH, Lc2=0μH, Ls1=10μH, Lp1=53μH, Cs1=1.2μF, Cp1= 0.72μF,

(b) Inverter output in unified PSM with dual control (Rc1 =Rc2=500mΩ, Lc1=2μH, Lc2=0μH, Ls1= 110μH, Lp1=53μH, Cs1=1.2μF, Cp1=0.72μF, Ls2=100μH, Lp2=50μH, Cs2=1.1μF, Cp2=0.68μF).

(c) Inverter output in symmetrical PSM with magnitude control (Rc1= Rc2= 500mΩ, Lc1=0μH, Lc2=2μH, Ls1=100μH, Lp1=50μH, Cs1=1.1μF, Cp1=0.68μF, Ls2=110μH, Lp2=53μH, Cs2=1.2μF, Cp2=0.72μF).

(d) Inverter output in unified PSM with dual control (Rc1=Rc2= 500mΩ, Lc1=0μH, Lc2=2μH, Ls1= 100μH, Lp1=50μH, Cs1=1.1μF, Cp1=0.68μF, Ls2= 10μH, Lp2=53μH, Cs2=1.2μF, Cp2=0.72μF).

Delay, driver delay, connection deviations, and modulator randomness, the output characteristics are unique in the individual inverter of the parallel system. The synchronized phase is significant for different output characteristics to accomplish magnitude CSC. Finally, it is concluded from simulation and experiment that the unified PSM is superior to the symmetrical PSM for resonant inverters in parallel connection. In addition to optimized

synchronization, a controllable phase angle is also accomplished by the unified PSM. In phasor transformer-based CSC, a controllable phase is indispensable to achieve reactive current control in parallel system. Therefore, the advanced CSC algorithm is easy to be implemented by the proposed PSM for the parallel single-stage resonant inverter. On the other hand, compared with the two-stage resonant inverter, the proposed modulation and control scheme achieves the same control capability in the single-stage resonant inverter with the simpler power circuit and hence achieves lower cost.

7. CONCLUSION AND FUTURE WORK

HFAC PDS attracts more and more attention from both industry and academia. It is complicated to implement output synchronization for the HFAC power source formed by the resonant inverter in parallel connection. In order to achieve a good load sharing and minimize circulation current, a unified PSM was presented to simultaneously regulate the magnitude and phase of the single-stage resonant inverter. The ac analysis of phase angle demonstrates the phase sensitivity to component parameters, and the significance of a phase controller is testified by phase sensitivity analysis. The typical waveforms in steady and transient states demonstrate the feasibility of the unified PSM. Moreover, the operational scope of the phase controller is determined by ZVS and THD conditions. The simulation and experiment further verify the theoretical analysis in steady and transient states. An experiment prototype constructed by two resonant inverters in parallel connection has been established with an operating frequency of 25 kHz.

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