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Optimization of FIR digital filter using low power MAC

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***Abstract* — In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit that consumes low power is always a key to achieve a high performance digital signal processing system. Finite impulse response (FIR) filters are widely used in various DSP applications.The purpose of this work is, design and implementation of Finite impulse response (FIR) filter using a low power MAC unit with clock gating and pipelining techniques to save power.**

***Keywords*— MAC, Low Power, Glitch Reduction, Clock Gating, Latch Based Design, Pipelining.**

I. INTRODUCTION

Finite impulse response(FIR)filters are widely used in various DSP applications.This paper describes an approach to the implementation of low power digital FIR filter based on field programmable gate arrays (FPGAs).The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches.

Firstly, a single MAC unit is designed, with appropriate geometries that give optimized power, area and delay. Similarly, the N no. of MAC units are designed and controlled for low power using a control logic that enables the each stage at appropriate time. Multiply –Accumulator unit has become one of the essential building blocks in digital signal processing applications such as digital filtering,speech processing, Video coding and cellular phones.

II. MULTIPLY-ACCUMULATOR UNIT

A conventional MAC unit consists of multiplier and an accumulator that contains the sum of the previous consecutive products. A variety of approaches to the implementation of the multiplication and addition portions of the MAC function are possible. In Fig.1we proposed design methodology for the structure of MAC unit which is extended to handle two's complement multiplication. This signed MAC unit consists of multiplying 2 values, then adding the result to the previously accumulated value, which must then be restored in the registers for future accumulations. We choose 12 bit precision input bus with along with this we add one extra sign bit so in total at input side 13 bit is applied and output is 31 bit precision.

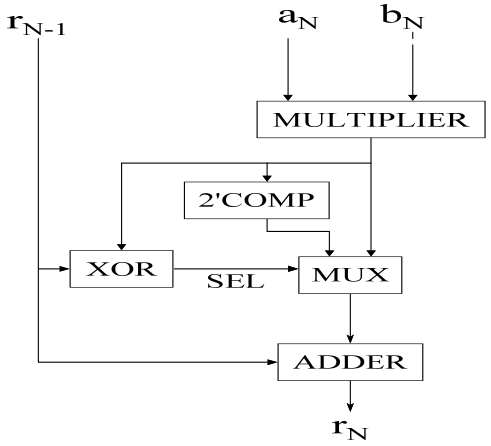

Fig.1 Basic structure of MAC unit

III. FIR FILTERS

Finite impulse response (FIR) filters are widely used in various DSP applications. Finite Impulse Response (FIR) filter is implemented as a series of multiply and accumulate operations on a programmable Digital Signal Processor (DSP). Fig. 2 shows the direct form of digital FIR filter. In the direct form, there are delay units between multipliers. The output of a FIR filter is described by the following equation:

$$y[n] = a_0 x[n] + a_1 x[n-1] + ... + a_{N-1} x[n-N] \quad (1)$$

At a time, the present filter input, x(n), and N-1 previous samples of the input are fed to each multiplier input, and the filter output y(n) is the sum of product of every multiplier. x[n] is the input signal.y[n] is the output signal. a_i are the **filter coefficients**, also known as **tap weights**, that make up the impulse response.The output y of a FIR system is determined by convolving its input signal x with its impulse response a .

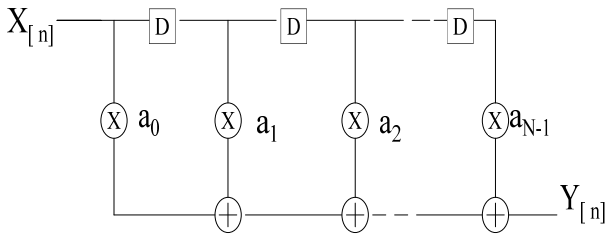

Fig.2 Direct form of N tap FIR filter

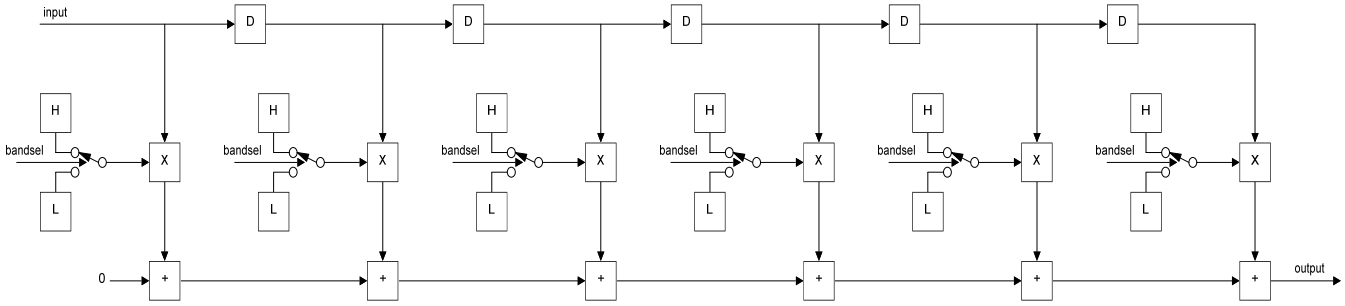

Fig.3 Basic structure of 6 tap FIR filter

IV. 6 TAP FIR FILTERS

In this paper we propose a design of 6 tap FIR filter as shown in fig 3. From this figure 3 the input is delayed and given to multiplier each multiplier gives products corresponding to different filter coefficients and all these products are accumulated and give FIR filter output. We used H and L coefficient from DB3 wfilter from matlab and suitably convert these values into binary for input to design filter else we can give any coefficient to this filter. The RTL schematic of 6 tap digital FIR filter is shown in figure 5.

V. DYNAMIC POWER DISSIPATION

Dynamic power makes up a large portion of the total amount of power consumed by an FPGA design. In CMOS circuits, the dominant source of power dissipation is the dynamic power dissipation. Whenever the logic level changes at different points in the circuit because of the change in the input signals the dynamic power dissipation occurs. Dynamic power is determined by the following equation.

$$P_D = \alpha C V^2 f \qquad (2)$$

Where alpha is the switching activity factor, C is the capacitance, V is the supply voltage, and f is the clock frequency. In addition to voltage and physical capacitance, switching activity also influences dynamic power consumption. A chip may contain an enormous amount of physical capacitance, but if there is no switching in the circuit, then no dynamic power will be consumed. The data activity determines how often this switching occurs.

VI. LOW-POWER DESIGNS

Design for low power has become increasingly important in a wide variety of applications, including digital signal processing , mobile computing , high performance computing, and high-speed networking. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. Above equation shows that the dynamic power consumption is proportional to switching activity. Therefore, minimizing switching activity can effectively reduce the power dissipation without impacting the circuit performance.

The activity can be reduced with different methods and at different levels.

A. Clock Gating

Clock gating, which is probably one of the most well-known low-power techniques, is very effective in reducing the power consumption in digital circuits. The goal of this technique is to disable or suppress transitions from propagating to parts of the clock path (i.e., flip-flops, clock network, and logic) under a certain condition computed by clock-gating circuits. The savings are mainly due to the switching capacitance reduction in the clock network and the switching activity in the logic fed by the storage elements because unnecessary transitions are not loaded when the clock is not active.

B. Glitch Reduction

For arithmetic circuits, a large portion of the dynamic power is wasted on un-productive signal glitches. Glitches are due to converging combinatorial paths with different propagation delays. Signal glitching refers to the transitory switching activity within a circuit as logic values propagate through multiple levels of combinational logic.

VII. CLOCK GATING OF LATCH BASED DESIGN

In some applications, latch-based designs are preferred to D Flip Flop (DFF)–based designs. The basic concept is that a DFF can be split into two latches, and each one is clocked with an independent clock signal.

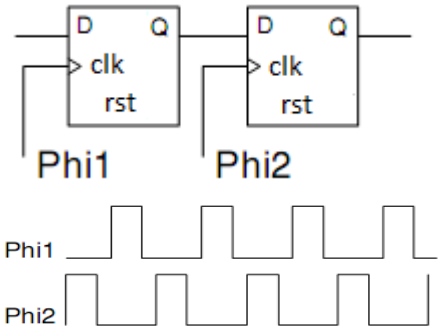

Fig.4 Clock gating of latch-based design

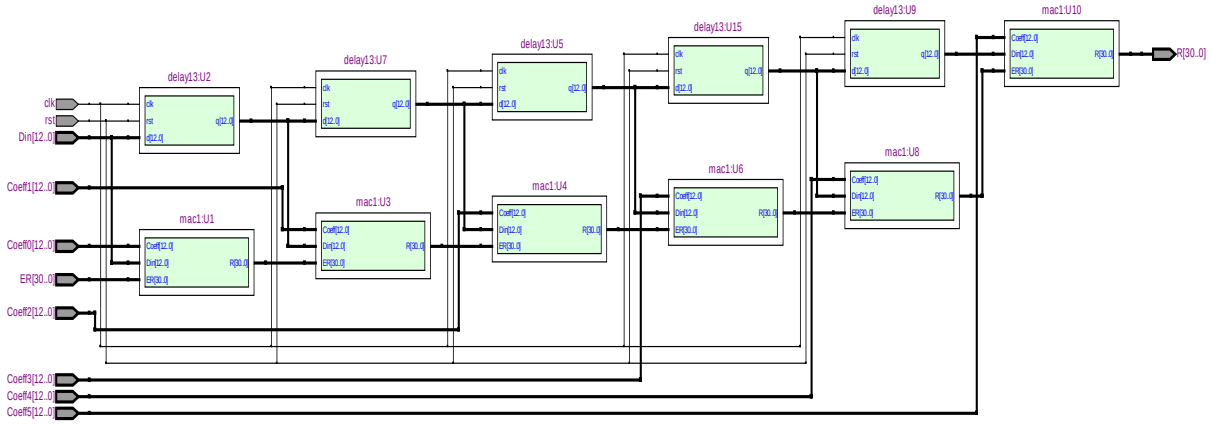

Fig.5 RTL schematic of original 6 tap FIR filter

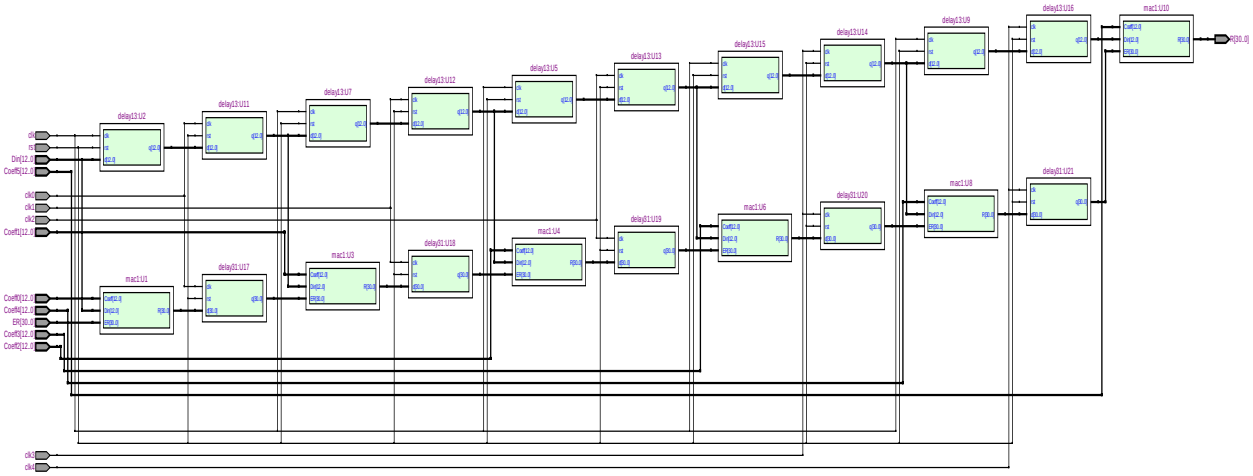

Fig.6 RTL schematic of latch based 6 tap FIR filter

The two clocks are nonoverlapping clocks as presented in Figure 4. Combinational network is usually inserted between the two latches to build a pipelined data path. The main advantage is that this kind of design supports greater clock skew before failing than a similar DFF-based design. The second advantage is that time borrowing is achieved naturally in the pipelined data path.Latch-based designs with several non-overlapping clocks have been proposed and they have seen to be more reliable at very low supply voltage. Conservative non-overlapping clocks are used, i.e. a Phi1 clock pulse for the first period of the master clock CK and a second Phi2 pulse for the second period of the master clock. Figure 6 shows the RTL schematic of latch based 6 tap FIR filter.

VIII. PIPELINING

Pipelining is a simple and effective way of reducing glitching, and hence minimizing power consumption. Pipelining reduces the critical path, but leads to a penalty in terms of an increased latency. The speed of a DSP architecture (or the clock period) is limited by the longest path between any 2 latches, or between an input and a latch, or between a latch and an output, or between the input and the output. This longest path or the "critical path" can be reduced by suitably placing the pipelining latches in the DSP architecture. In an M-level pipelined system, the number of delay elements in any path from input to output is (M-1) greater than that in the same path in the original sequential circuit.

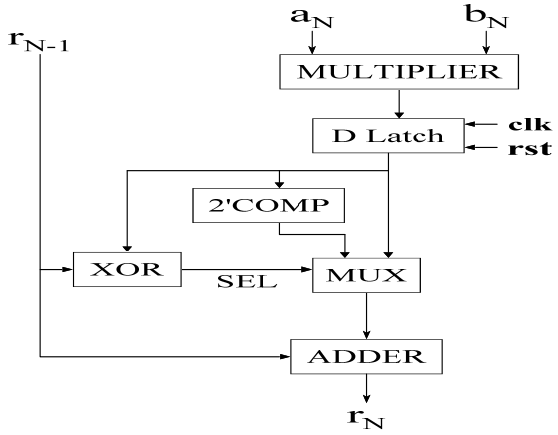

Fig.7.Basic structure of 2 level pipelined MAC

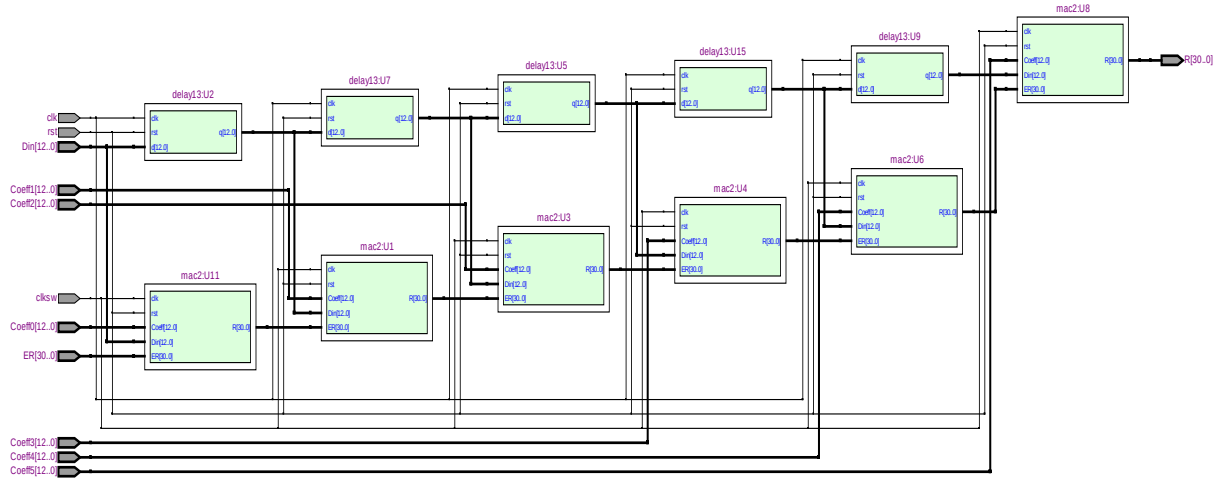

Fig.8.RTL schematic of 6 tap FIR pipelined filter

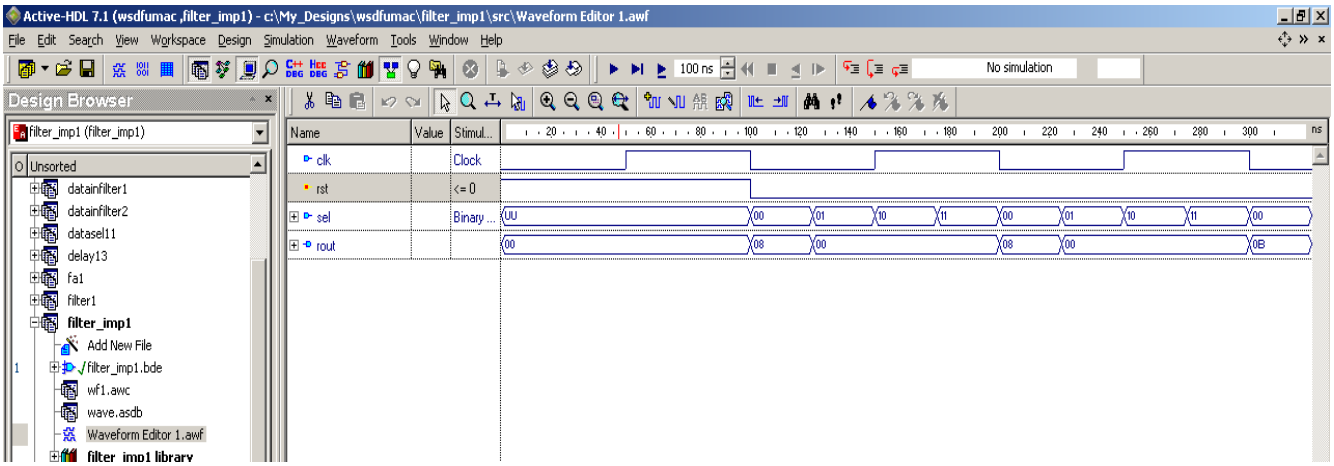

Fig.9.Simulation results for original 6 tap FIR filter

Figure 7 shows structure of MAC unit in which 2 levels pipelined technique is implemented. A latch is inserted between multiplier and adder. When sample speed does not need to be increased, these techniques can be used for lowering the power consumption. This 2 level pipelined is used to design 6 tap FIR filter. Previous studies have shown that power dissipation caused by glitching can make up a significant amount of total dissipated power. An important technique for reducing FPGA power consumption is to reduce the amount of signal glitching within the circuit. Pipelining is one technique for reducing signal glitches. A pipelined design has less logic between registers and therefore is less prone to glitching. Pipelining an FPGA design can come at little or no cost since i/p-o/ps are included in every FPGA logic block and often go unused.Fig.8 shows the RTL schematic of 6 Tap pipelined FIR filter.

IX. Simulation And Results

A FIR filter scheme suitable for unsigned and signed computations is presented in this paper. Low power designs for 6 Tap FIR filter using latch based and pipelining techniques are implemented. These filters are designed using MATLAB and developed VHDL code. Simulation is performed using Active-HDL and functional verification is carried out using Altera Quartus II and, FPGA implementation on Cyclone. Figure 9 shows simulation result performed in Active-HDL for 6 tap FIR filter. Simulation result of latch based FIR filter is shown in figure 10.Whereas figure 11 shows simulation result of pipelined FIR filter in Active HDL.Using finite state machine input values and filter coefficients have given to this digital FIR filter.

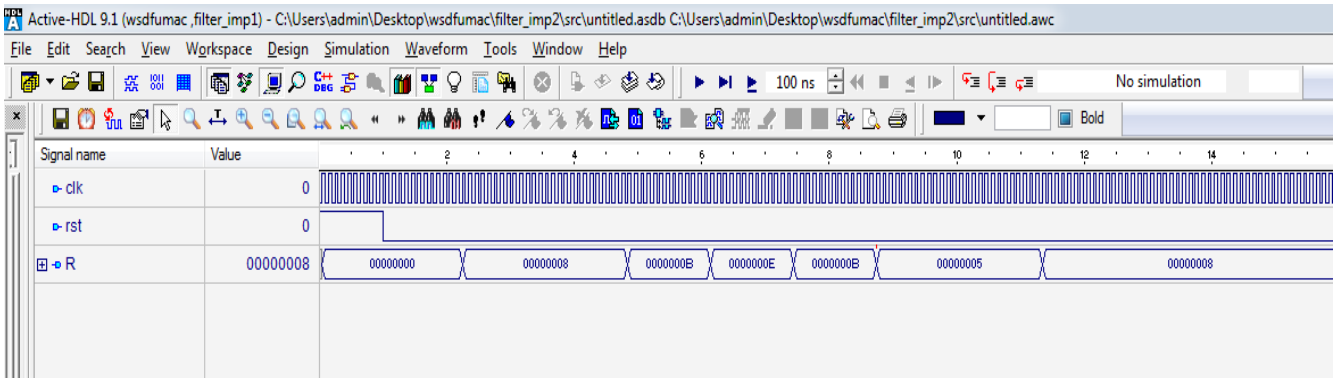

Fig.10 Simulation results for Latch Based 6 tap FIR filter

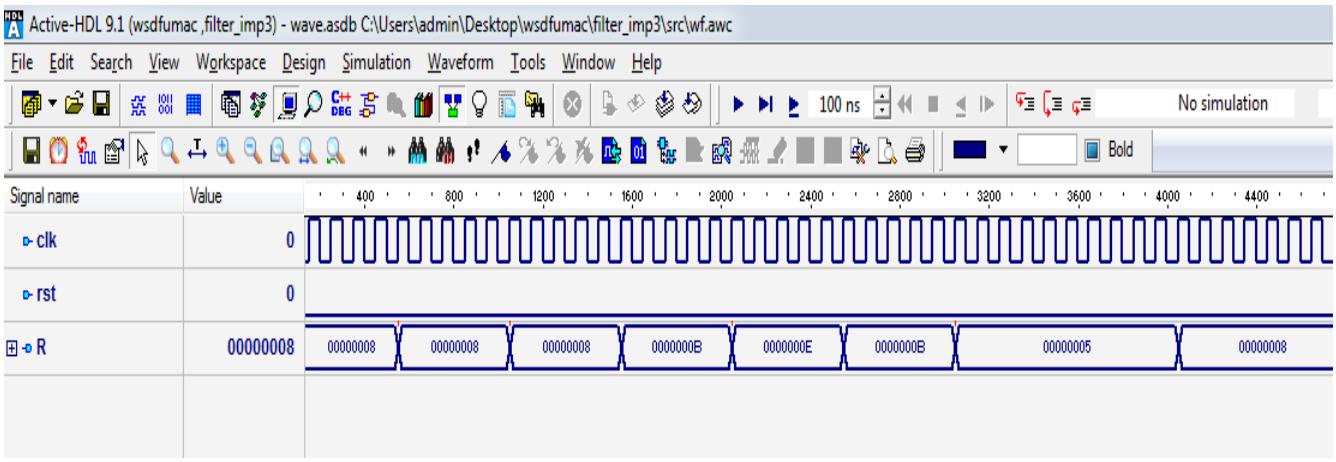

Fig.11. Simulation results for 6 tap pipelined FIR filter

TABLE I
POWER ANALYZER SUMMARY

6 tap FIR filter	Core dynamic thermal power dissipation
Original Filter	21.40mW
Latch Based Filter	1.73mW
Pipelined Filter	1.09mW

It can be seen that dynamic power consumption is decreased through the use of two techniques; latch based clock gating and pipelining of original 6 tap FIR filter as shown in table I. The proposed FIR filters have been synthesized and implemented using Altera Quartus II FPGA and power is analyzed using Power Play Power Analyzer Tool.

X. CONCLUSION

Design for low power 6 tap FIR filter has been presented in this paper. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. The basic building blocks for the MAC unit are identified and each of the blocks is analysed for its performance. Power is calculated for the blocks. 1-bit MAC unit will be designed with enable to reduce the total power consumption based on above proposed techniques. Active-HDL together with Altera Quartus II tool is used effectively to model dynamic transient signal activity and produce accurate power consumption estimation. It is seen by above results that Latch based design can reduce the dynamic power consumption by 92% and pipelining reduces that up to 95%.

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