ISSN:2231-0711
www.ijcset.net

A Frequency Synthesis of All Digital Phase Locked Loop

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***Abstract* — All Digital Phase locked loops (ADPLL) plays a major role in System on Chips (SoC). Many EDA tools are used to design such complicated ADPLLs. It operates on two modes such as frequency acquisition mode and phase acquisition mode. Frequency acquisition mode is faster compared to Phase acquisition, hence frequency synthesis is performed. The CMOS technology is used to design such a complex design in Micron Technology. The frequency of the ADPLL is synthesized using feed forward compensation techniques. All the parameters of ADPLL (Power consumption, area, locking time) are obtained using 0.18µm technology. The synthesis of ADPLL with Digitally Controlled Oscillator (DCO) and modified Digitally Programmable Delay Element (DPDE) are done and it is found that ADPLL with DPDE consumes less power compared to ADPLL with DCO.**

Keywords- All digital Phase locked loops(ADPLL), EDA tool, CMOS technology , frequency synthesis, Digitally Controlled Oscillator(DCO), ring oscillator, Digitally Programmable Delay Element (DPDE).

I. INTRODUCTION

A Phase-Locked Loop (PLL) is a closed-loop frequency-control system based on the phase difference between the input clock signal and the feedback clock signal of a controlled oscillator. The main blocks of the PLL are the phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO), and counters, such as a feedback counter (M), a pre-scale counter (N), and post-scale counters(C).

Analog approaches are adopted to design PLLs. But it is difficult to integrate an analog PLL into a noisy SoC environment. Therefore, it becomes popular to digitalize the implementation of the loop filter and oscillator circuits in PLLs [2], [3].This kind of PLLs is named as All-Digital Phase-Locked Loop (ADPLL).

Compared with the traditional analog PLLs, ADPLL has several advantages. First, most of the signals in the ADPLLs are digital formats. Thereby, the ADPLLs have higher immunity to switching noise. Second, the ADPLLs can be implemented by electronic design automatic (EDA) tools. This can reduce design time greatly. Third, the analog filter is replaced with digital filter. The large area for the capacitors in the analog filter is saved. Therefore, the ADPLL is more readily scaled down in size when new fabrication processes are utilized. Fourth, the frequency of the digitally controlled oscillator (DCO) is tuned by digital codes. So ADPLLs are much easier to achieve fast frequency acquisitions [1].

To reduce the power consumption, the SoC processor will enter the sleep mode when it is not in use. In the sleep mode, the processor will turn off several parts of the processor. This may include turning off the PLL. When the SoC processor exits the sleep mode PLL should provide the processor with the correct clock as soon as possible. So, designing a fast locking PLL is very important for a SoC processor. Usually, there are several frequency search algorithms used in ADPLL. One of the typical methods is adjusting the PLL's loop bandwidth dynamically [4], [5]. This method is very common in fast locking charge pump PLLs [6].

In this paper, a fast locking ADPLL via feed-forward compensation technique is described. The proposed ADPLL has two operation modes which are frequency acquisition mode and phase acquisition mode. In frequency acquisition mode, a feed-forward compensation structure is activated. It takes two reference cycles to estimate an ADPLL parameter which is called here, and predicts the desired code. The predicted code is directly sent to the DCO. Then the ADPLL enters the phase acquisition mode, a PLL is activated to eliminate the remaining frequency error. The Microwind, EDA software is used to design any complicated IC in back-end chip design. For any circuit design steps to be followed are Circuit implementation, Simulation, Transistor level extraction and Circuit verification. After completing all the above processes we get an imaginary circuit layout.

This paper is organized as follows. The feed-forward compensation algorithm is proposed in Section II. In Section III, the structure and operation of the proposed ADPLL is introduced. Implementation of ADPLL is described in Section IV. Power and Delay Analysis of ADPLL is given in Section V, and conclusions are given in Section VI.

II. FEED FORWARD COMPENSATION ALGORITHM

When the code W is assigned to tune the DCO, the DCO frequency is 'f'. 'F' is the corresponding value sensed by the modified frequency divider (MDIV). The operation of the MDIV will be explained in Section IV. Simply speaking, the MDIV counts by the rising edge of the DCO clock when the reference clock is low level. When the reference clock rises, the value of the counter

in MDIV is saved as F. In the following, the subscripts on the symbols f and F accord with the subscript on the symbol W. So, when two codes W1 and W2 are assigned to tune the DCO successively, the corresponding frequencies of the DCO are f1 and f2. F1 and F2 are the corresponding values sensed by the MDIV. The relation between the sensed value and the frequency of the DCO is given in (1)

$$F = \frac{f}{2f_{\text{ref}}} \quad (1)$$

Where f_{ref} is the reference clock frequency. Therefore, the frequency error between and can be represented by the difference between F1 and F2

$$F_1 - F_2 = \frac{(f_1 - f_2)}{2f_{\text{ref}}}. \quad (2)$$

In many DCO designs, f1 and f2 can be defined as (3)

$$f_1 = f_{\min} + K_o \bullet W_1, \quad f_2 = f_{\min} + K_o \bullet W_2 \quad (3)$$

Where K_o is the DCO gain measured in megahertz, and f_{min} is the minimum frequency of the DCO. Combining (2) with (3), the parameter K_f can be obtained by (4)

$$K_f = \frac{2f_{\text{ref}}}{K_o} = \frac{W_1 - W_2}{F_1 - F_2}. \quad (4)$$

Then (4) can be rewritten as (5)

$$W_1 = W_2 + K_f \bullet (F_1 - F_2). \quad (5)$$

Because of the MDIV which will be described later, the stored value of F is M/2 when the ADPLL is frequency locking. M is the frequency divider ratio.

In (5), F1 replacing with M/2, and W can be calculated by (6) equation

$$W_{\text{locked}} = W_2 + K_f \bullet \left(\frac{M}{2} - F_2\right). \quad (6)$$

From (6), it is seen that the ADPLL with the proposed algorithm can achieve a fast frequency locking when the values W_2 and are known. The code W_2 is generated by the ADPLL itself. The value is set to the ADPLL before the ADPLL works, and the value is sensed by the MDIV, so these values can be obtained easily. The value which is the most difficult to obtain is K_f. From (4), it is seen that the parameter K_f is PVT dependent. So it is better to recalculate the value of for every initialization of the ADPLL.

III. STRUCTURE AND OPERATION OF ADPLL

The ADPLL, shown in Fig. 1, includes a phase/frequency detector (PFD), a MDIV, a loop control (LC), a ring type DCO, a first-order digital loop filter (DLPF), and a P2D. The stage of the DCO in the ADPLL is five, so the DCO can provide five clocks whose phases are different. The five clocks are named as clk[0], clk[1],clk[2],clk[3] & clk[4].

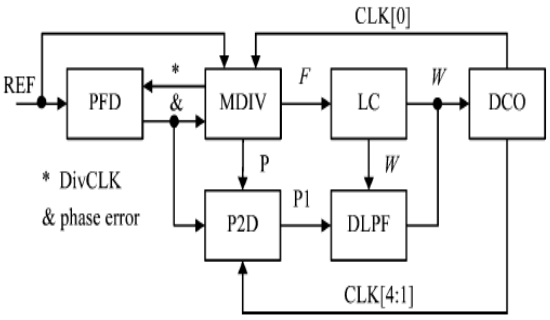

Fig. 1.Structure of the ADPLL

A detailed diagram of the ADPLL architecture is shown in Fig.2, together with the signals reflected in the pseudo code that models the ADPLL behaviour [3]. The DCO contains fours capacitor banks that are used with three operational modes: process, voltage, and temperature (PVT) variations, acquisition, and tracking. The first two are used during frequency settling and are frozen afterwards. The frequency of the DCO output clock CKV signal is controlled by the Oscillator Tuning Word (OTW) , which is a fixed-point digital word, i.e., OTW = OTW_I - OTW_F ,with the fractional part utilized in tracking mode only. The OTW-to-fv dependency is in general nonlinear because of the *LC*-tank-based structure of the DCO.

The slope of the characteristic represents the DCO gain, K_{DCO} (in Hz/LSB), and the step size determines the DCO frequency resolution. It indicates a frequency deviation of K_{DCO} (Hz) from the DCO effective centre frequency f_0, when the OTW is changed by 1 LSB. The finest frequency resolution is utilized when the ADPLL is in tracking mode. Specifically, for 90-nm CMOS and small frequency perturbations around 1.8 GHz, the K_{DCO} is about 12 kHz/LSB. However, further resolution improvement is achieved by exercising the fractional part of OTW to dither the tracking bank varactors through high-speed dithering, as shown in Fig.1.

The ∑Δ modulator is implemented as a second-order multistage noise-shaping (MASH)-type structure and is described in PVT variations as well as the DCO variable oscillation frequency, are a set of factors that highly affect K_{DCO} in an uncertain way. To minimize the ADPLL dependency on the DCO gain variation, K_{DCO} is algorithmically estimated as K_{DCO}, and the DCO gain is normalized to the stable reference frequency f_R, [3].The ADPLL phase-detection mechanism is based on cycle (i.e., phase) accumulation performed at the rising edges of the CKR and CKV clocks.

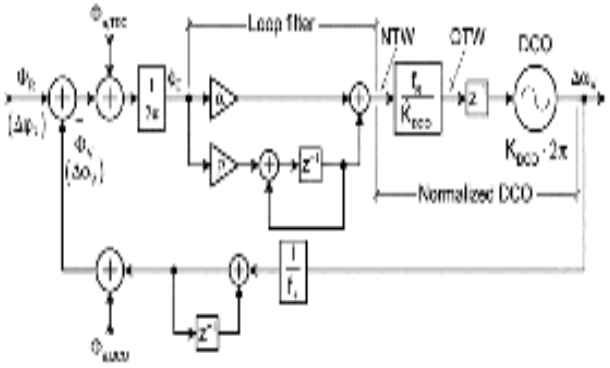

Fig. 2.Z domain ADPLL model

IV. IMPLEMENTATION OF ADPLL

The design of such complex PLL digital circuit in PCB is very difficult and only technical will be able to do the connections. But using XILINX and Tanner tools we can easily design any circuits and we can simulate for various values of input supply voltage and wire length. Various front end tools are available to draw the circuit with number of components.

A. Phase Frequency Detector(PFD)

The Phase Frequency Detector has the input vdd which is applied to the flip-flops and the corresponding clock signals given to the resettable D flip-flops. PFD detector is used to find the phase and frequency difference between the input signals and feedback signal from MDIV. It compares the two signals and detects the phase and frequency. The functional verification of PFD is done by using Xilinx tool.Two pulse voltage sources are used as the input signal of PFD, one is input signal of whole ADPLL and the other is treated as the feedback from MDIV. If the REF falls first, the signal UP is high level and the signal DOWN is low level. It indicates that the REF leads the MDIV (or vice versa). If the signals UP and DOWN are both high levels, the two signal both reset to low levels by a feedback reset signal.

B. Modified Frequency Divider(MDIV)

The MDIV circuit consists of the multiplexer it enables the DIVCLK, with the help of REF signal it reset the DIVCLK using AND, OR gates. It is used to generate the signal parameter 'F'. Hence the frequency is locked in 2 reference clock cycle. The functional verification of MDIV is done by using Xilinx tool.

C. Loop Control(LC)

The loop control performs two operations when the ADPLL is initialized. First, the LC calculates W_0. Second, it generates based on $W_{locked,}$ by (f1-f2), the algorithm needs two reference cycles to obtain the parameter. From the input MDIV the values, reference cycle are obtained in W_1 and W_2 code.

D. Digitally Controlled Oscillator(DCO)

The DCO circuit consists of a delay cell. The cell consists of CMOS transistor. It generate five clock which are named as CLK [0] - CLK [4], respectively. The functional verification of DCO is done by using Xilinx tool. The DCO is the combination of a digital-to-analog converter (DAC) and a voltage controlled oscillator (VCO). Based on the input code (W), the DAC converts the code to the voltage. Then voltage controls the frequency of the VCO is the same and can act as resistors. So the voltage increases with the increase of the current and fed back to the MDIV and P2D.

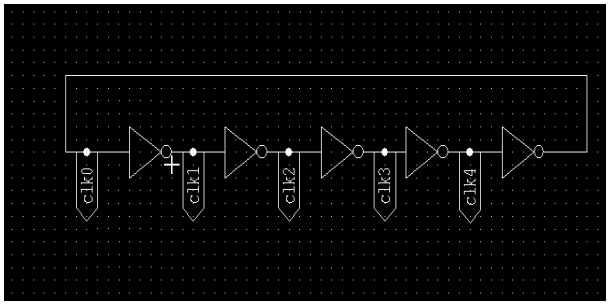

Fig. 3. Stucture of DCO

E. Digitally programmable delay element(DPDE)

DPDE are required to be monotonic and low power. A low power DPDE monotonic delay characteristic is proposed. To avoid direct current in an output transistor, an extra inverter is introduced. A set of control transistor is connected in series. It consists of load capacitance (C_L), charging network (CN) that provides charging current (IC) and discharging network (DN) that provides discharging current (ID). The delay "t_d" depends on the load capacitor, charging current and the voltage swing across capacitor, V_{sw}.

$$T_d = (C_L V_{sw}) / I$$

Delay control is often accomplished by adjusting I, C_L or V_{sw}. The fig 7 shows the digitally programmable delay element.

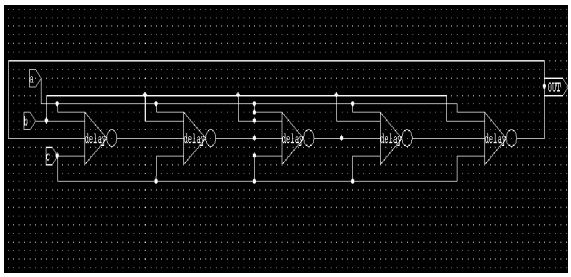

Fig. 4.Structure of DPDE

F. Ring oscillator(RO)

The ring oscillator is a member of the class of time delay oscillators. The fig.9 shows the structure of ring oscillator. A time-delay oscillator consists of an inverting amplifier with a delay element between the amplifier output and its input. The amplifier must have a gain of greater than 1.0 at the intended oscillation frequency. Consider the initial case where the amplifier input and output voltages are momentarily balanced at a stable point. A small amount of noise can cause the amplifier output to rise slightly. After passing through the time-delay element, this small output voltage change will be presented to the amplifier input. The amplifier has a negative gain of greater than 1, so the output will change in the direction opposite to this input voltage. It will

change by an amount larger than the input value, for a gain of greater than 1. The square wave will grow until the amplifier output voltage reaches its limits, where it will stabilize. A more exact analysis will show that the wave that grows from the initial noise may not be square as it grows, but it will become square as the amplifier reaches its output limits. The synthesis of ADPLL with Digitally Controlled Oscillator (DCO) and modified ring oscillator are done and it is found that ADPLL with ring oscillator consumes less power compared to ADPLL with DCO.

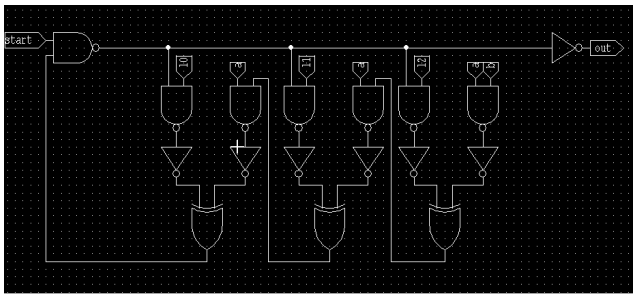

Fig .5.Ring Oscillator With Variable Delay

G. Digital Loop Filter(DLPF)

The circuit consists of the multiplexer and its enables W .when enable is high DPLF turns OFF the frequency modes. The code predicted by the LC (K_1 and K_2) is inserted into the DLPF. The functional verification of DLPF is done by using Xilinx tool. When the signal Enable (e) is high level, the code predicted by the LC output (W) is inserted into the integral path of DLPF, the input of the DLPF (out) keeps zero during the frequency acquisition mode. So, when the ADPLL enters the phase acquisition mode, the first code output is generated by DLPF. Then the following codes are decided by the sensed phase error.

V. POWER AND DELAY ANALYSIS

The power of the DCO, VRO and DPDE has been analyzed as shown in fig. 6. The power consumed by the proposed DCO is given by 10.15596mW. The power consumed by the proposed ring oscillator is given by 9.9012mW. The power consumed by the propose DPDE is 9.740202mW. The area of the DCO, VRO and DPDE has been shown in fig. 7. And the power delay product of DCO, VRO and DPDE has been shown in fig. 8. The ADPLL circuit takes some time period to generate the control bits to frequency and phase modes. The total time delay taken by the clock signals present in the circuit is given as 6.209ns.

TABLE 1.1 ESTIMATED PARAMETER ANALYSES

PERFORMANCE PARAMETER	DCO	RING OSCILLATOR	DPDE
POWER	10.16mW	9.90mW	9.74mW
AREA Of THE TRANSISTOR	358.4um	261.40um	325.8um
POWER DELAY PRODUCT	6.3452ps	1.3039ps	5.3452ps

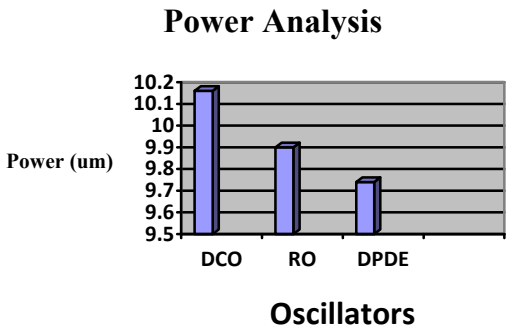

Fig .6.Power Result Analysis

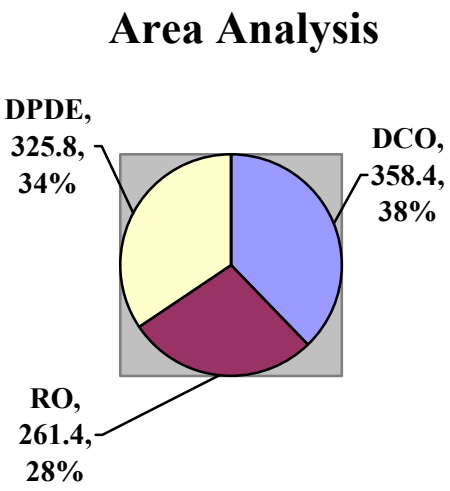

Fig .7.Area Analysis

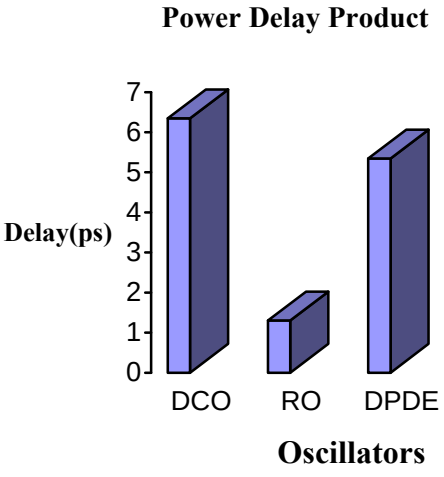

Fig .8.Power Delay Product Analysis

VI. CONCLUSION

The fast locking ADPLL ensures reduction of the locking time. The fast locking ADPLL is proposed with feed-forward compensation algorithm and reutilizes a frequency divider. The frequency range of the ADPLL is 4–416 MHz the measured results show that the ADPLL can complete frequency locking in 2 reference cycles, when locking to 376 MHz the corresponding frequency

locking time is three cycles. The phase locking time power consumption is 11.394mW. However, based on the simulation results, the much larger than the frequency locking times. The largest phase locking time is 19 reference cycles. So the major improvements are found to be possible to enhance the performance of the proposed ADPLL. In DCO block modifying with Digitally Programming Delay Element (DPDE), the power can be reduced, and it used in low power application. In DPDE block, it reduces the error frequently in phase and frequency acquisition mode. Thus the fast and effective locking time can be achieved. In future delay can be reduced the delay and increasing the speed.

ACKNOWLEDGEMENT

The authors thank the Management and Principal of Sri Ramakrishna Engineering College, Coimbatore for providing excellent computing facilities and encouragement

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