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A Low power 50 nm Technology Based CMOS Inverter with Sleep Transistor Scheme

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***Abstract*— This paper proposes a sleep transistor based minimum size inverter in BSIM4.3.0, 50nm CMOS technology with supply voltage of 1V, power dissipation of 46.28nW at 0.502V and maximum drain current of 70nA. The operating frequency is 1GHz. The disadvantage is decrease in voltage swing by 15% compared to the conventional CMOS Inverter of the same size, whereas the power dissipation is only 1.117% of the power dissipated by classical CMOS inverter and operating frequency is almost 2 times. It is able to satisfy the low standby power requirement and simultaneously high performance during the active mode for many mixed signal applications.**

***Keywords*— Sleep transistor, 50nm, BSIM4.3.0, Voltage Swing.**

I. INTRODUCTION

The minimum channel length of the transistor will be scaled down to 30 nm in 2012 [15] according to the roadmap of semiconductors. In addition to this downscaling, today's System-On-Chip (SoC) [6] trends forces analog and mixed-signal integrated circuits to be integrated with complex digital processors and memory on a single chip. The mixed signal integrated circuits therefore should dissipate as low power as possible.

BSIM4, [8, 14] as the extension of BSIM3 model, addresses the MOSFET physical effects into sub-100nm regime.

The classical CMOS inverter shown in Fig.1 is designed at 50nm and analysed; the results are shown in Table 1. The general equation of I_{ds} for both triode and saturation region for sub 100nm device is given in (1) [14].

$$I_{ds} = \frac{I_{dsp}.NF}{1+\frac{R_{ds}.I_{dsp}}{V_{dseff}}}\left[1+\frac{1}{C_{clm}}ln\left(\frac{V_A}{V_{Asat}}\right)\right].\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADIBL}}\right).\left(1+\frac{V_{ds}-V_{dseff}}{V_{ADITS}}\right).\left(1+\frac{V_{ds}-V_{dseff}}{V_{ASCBE}}\right) \quad \text{.....(1)}$$

On solving with substitution and elimintion the equation turns out to be (2).[5, 4, 3, 14]

$$I_{ds} = W v_{sat} C'_{ox}\left(V_{gs,n,p} - V_{th,n,p} - V_{ds,sat}\right) \quad (2)$$

Where, W = Width

$$v_{sat} = \mu_{n,p}\frac{dV(y)}{dy} \quad (3)$$

$$C_{ox} = C'_{ox}.W.L \quad (4)$$

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (5)$$

$$\varepsilon_{ox} = 3.97\varepsilon_0 \quad (6)$$

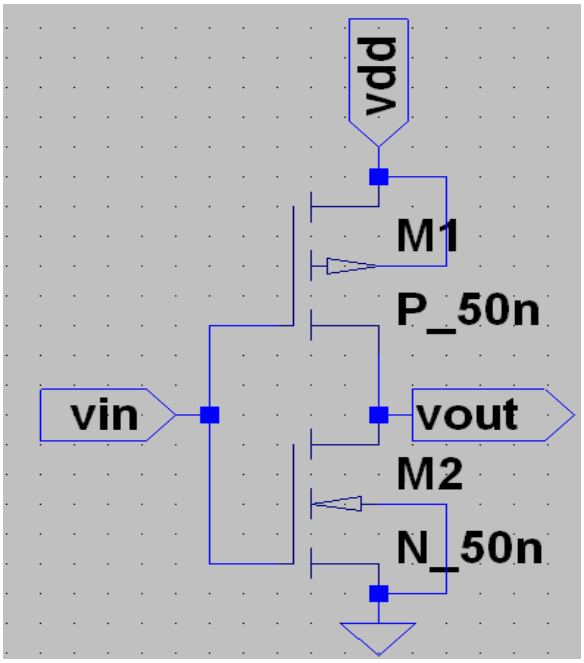

Fig.1, Classical 50nm CMOS Inverter

$$V_{th} = V_{th,L} + \gamma_B\left[\frac{N_{sub}}{N_{eff}}(2\varphi_F) - V_{bs}\right]^{\frac{1}{2}} - \gamma_A\frac{N_{sub}}{N_{eff}}(2\varphi_F)^{\frac{1}{2}} - \frac{bt_{ox}}{d_1}[2(\emptyset_{bt} - V_{bs} + V_{ds})]\exp\left(-\frac{\pi L}{4d_1}\right) \quad (7)$$

$$d_1 = \left(\frac{2\varepsilon_{si}}{q.N_{eff}}\right)^{\frac{1}{2}}(2.\varphi_f)^{\frac{1}{2}} \quad (8)$$

$$\emptyset_{bt} = \frac{kT}{q}ln\left(\frac{N_{sub}N_{eff}}{n_i^2}\right) \quad (9)$$

$$\varphi_F = \frac{kT}{q}ln\left(\frac{N_{eff}}{n_i}\right) \quad (10)$$

$$\gamma_A = \frac{\sqrt{2qs_{si}N_{eff}}}{C_{ox}} \quad (11)$$

$$\gamma_B = \frac{\sqrt{2qs_{si}N_{sub}}}{C_{ox}} \quad (12)$$

The simulation results for Fig.1 for DC and AC analysis are shown in Fig.2 and Fig.3 respetively. For voltage transfer characterstics (VTC) and drain current (I_{ds}) Equations (1) - (7) are used. Fig.2 shows that voltage swing is 100% and $(I_{ds})_{max}$ is 4.355μA at 0.511 V of input. Where as Fig.3 shows the FFT for the Fig.2 which show variation of V_{out} from -110 db to -6.5 db, I_{ds} -118.5 db to 288.5 db from 1 to 100KHz.

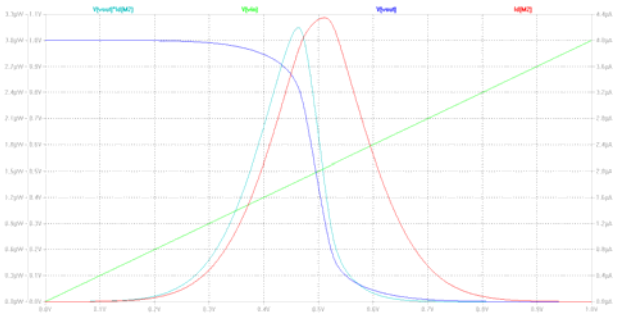

Fig.2, VTC of Classical 50nm cmos inverter showing full voltage swing, max current I_d(M2) at 0.511 V I/P, P_d 4.14μw at 0.463 V I/P), W_p/W_n = 2/1.

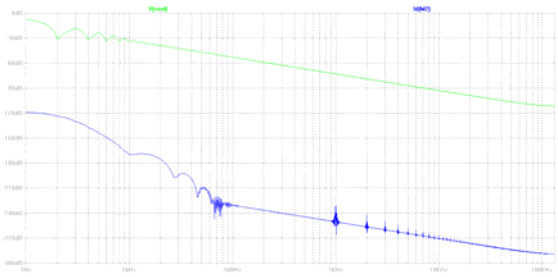

Fig.3, FFT for classical CMOS of 50 nm of V_{out} from -110 db to -6.5 db, I_{ds}-118.5 db to 288.5 db from 1 to 100KHz.

II. PROPOSED INVERTER

The classical CMOS [1, 2, 9, 13] circuit designed in 50 nm process although have reduced power dissipation than the higher technology for the same circuit but to further reduce the power dissipation in the same technology we use many methods out of which one method is using sleep transistors [10, 11, 12]. The proposed design with sleep transistors Fig.4 of minimum size when connected to V_{dd} and ground with main circuit of the same size as being used in the classical mode the current flowing through the drain I_{ds} Fig.6 and power dissipation Fig.7 of the circuit is reduced by many folds, the values are presented in Table 1 in detail for all the calculated parameters. The use of sleep transistors in the circuit although reduced I_{ds} and P_d, but the number of transistors used is 8 compared to 2 which will be responsible for increase in area. The voltage swing shown in Fig.5 is reduced by 15% which can be a big concern for the design. The mathematical equations used to calculate various parameters are shown in equation (13) to (21).[5,7]

$$P_d = CV_{dd}^2 f = V_{dd} \cdot I_{avg} \quad (13)$$

$$I_{avg} = I_d(\text{M2}) = I_{ds} \quad (14)$$

$$(\text{PDP})_{max} = P_{max} \cdot (T_{PHL} + T_{PLH}) \quad (15)$$

$$(T_{PHL} + T_{PLH}) = (R_n + R_p) \cdot C_{tot} \quad (16)$$

$$C_{tot} = C_{out} + C_{in} \quad (17)$$

$$C_{out} = C_{outn} + C_{outp} \quad (18)$$

$$C_{in} = C_{inn} + C_{inp} \quad (19)$$

$$C_{out} = C_{ox}' \cdot (W_n \cdot L_n + W_p \cdot L_p) \quad (20)$$

$$C_{in} = \frac{3}{2} C_{ox}' \cdot (W_n \cdot L_n + W_p \cdot L_p) \quad (21)$$

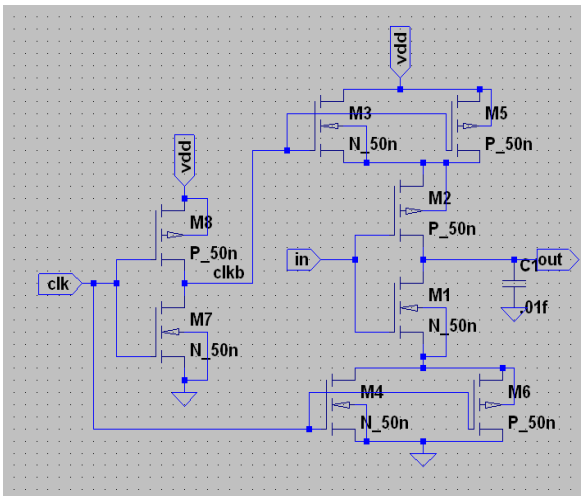

Fig.4, 50nm CMOS inverter with sleep transistors.

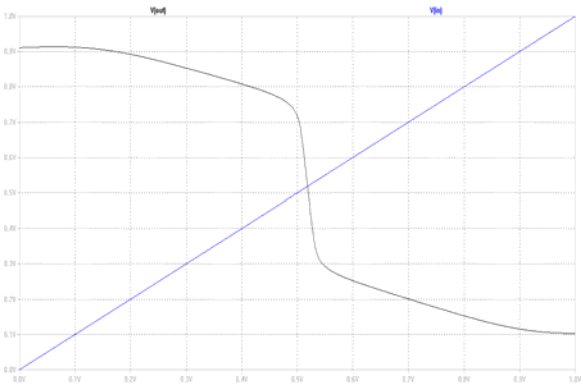

Fig.5, Voltage transfer characteristics of 50nm inverter 15 % decrease in voltage swing (102mv-915mV)

TABLE 1

S.No	Parameter	Classisical 50nm CMOS Inverter	Proposed 50nm sleep transistor Inverter
1.	Technology	50nm	50nm
2.	V_{dd}	1V	1V
3.	L_p = L_n	50nm	50nm
4.	W_n	50nm	50nm
5.	W_p	100nm	100nm
6.	$(W_p/W_n)_{sleep}$	N.A	1
7.	V_{tp}	-0.22V	-0.22V
8.	V_{tn}	0.22V	0.22V
9.	μ_p	0.0095	0.0095
10.	μ_n	0.032	0.032
11.	t_{ox}	14 Å	14 Å
12.	C_{ox}	25 fF/μm^2	25 fF/μm^2
13.	#Transistors	2	8
12.	Voltage Swing	100%	85%
13.	f	500MHz	1GHz
14.	$(I_{ds})_{max}$	4.355 μA	70 nA
15.	$(P_d)_{max}$	4.14 μW	46.28 nW
16.	T_{PLH}	120ps	90ps
17.	T_{PHL}	111ps	80ps
18.	Max PDP	956.34e-18	786.76e-20

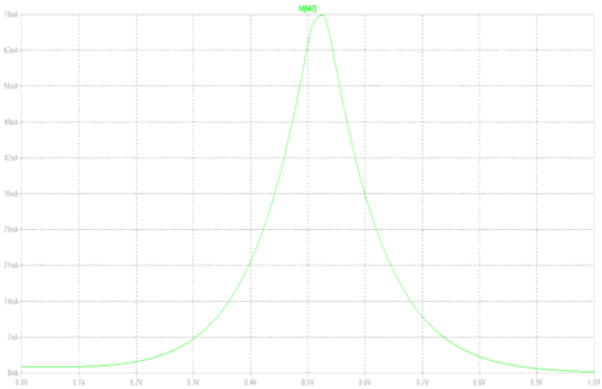

Fig.6, Drain Current through M2 for sleep Transistor Circuit Table 1

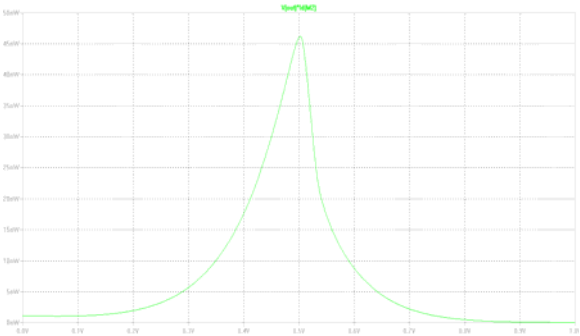

Fig.7, Power dissipation variation of sleep transistor inverter circuit

The power delay product (PDP) for both the circuits is calculated using equation (15) whereas the T_{PHL} and T_{PLH} are determined by transient analysis, the results for transient analysis is shown in Fig.8 the clock frequency is kept at 1Ghz for the circuit under consideration. The FFT curves for both AC and DC operation are plotted in Fig.9 and Fig.10 respectively. The FFT curve for AC analysis shows that the circuit is useful upto 10GHz although it is here operated only at 1GHz. The results of Fig.9 varies from -186.132db at 200 MHz to -6.26db at 1 GHz. The delay for the circuit is calculated from Fig.8.

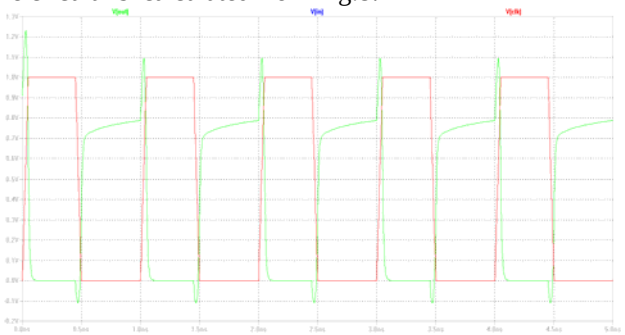

Fig.8, Transient behaviour of inverter at 1 GHz clock frequency

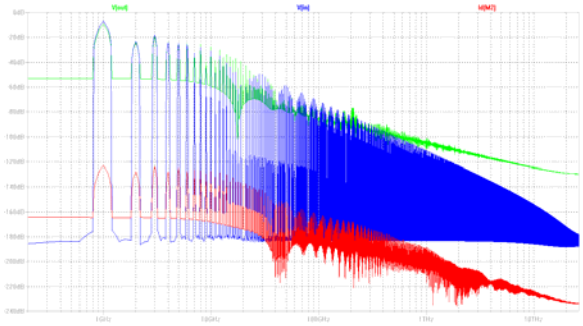

Fig.9, FFT Curves at 1GHz for I_d(M2), V_{out} , V_{in}

III. CONCLUSION

The CMOS inverter is one of the most important and used circuit in all analog as well as digital applications therefore the optimization of the inverter becomes very important. The circuit presented in this paper meets the requirement of reducing power dissipation up to 46.28nW which is far less than classical CMOS inverter in which it comes about 4.14μW. The reduction in $(I_{ds})_{max}$ is also from 4.335μA to 70nA, T_{PLH} is 90ps where as the value of T_{PHL} remains at 80ps. The biggest disadvantage of the design is 15% less voltage swing.

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