Design Optimization of High-Power Pulsed Mode IMPATT Oscillator: A Generalised Modelling on Sensitivity Analysis

Diptadip Chakraborty, Papia Bhattacharyya, Arijit Das, Milon Garai, Moumita Mukherjee
Centre for Millimeter-wave Semiconductor Devices and Systems (CMSDS), Institute of Radio Physics and Electronics, University of Calcutta,1, Girish Vidyaratna Lane, Kolkata 700009, West Bengal, India

***Abstract*— An optimized design of pulsed-mode Si double - drift IMPATT at W-band is presented in this paper. The design is made realistic by incorporating physics –based modelling and experimentally obtained material parameter data. For the first time, the authors have made a sensitivity analysis to study the effects of variation of critical design parameters on the high-frequency performance of the devices. The authors have studied the effects of variation of junction temperature on the device characteristics within a range of 300K-600K. A generalized physics-based drift-diffusion simulator is developed to study the optimized performance of the device.**

***Keywords*— Silicon IMPATT, Double-Drift device, Sensitivity modelling, pulsed device, elevated junction temperature.**

I. INTRODUCTION

IMPATT diodes have emerged at the end of the 20th Century, as most powerful solid-state sources of microwave and millimeter-wave, covering a wide range of frequency spectrum. The reported frequency range of IMPATT oscillators extends from below X Band (6 GHz) to the sub-millimeter wave region. IMPATT is an acronym for IMPact Avalanche Transit Time (IMPATT) diode, which reflects the mechanism of its operation. In its simplest form IMPATT is a reverse-biased p-n junction diode, in which an avalanche of electron-hole pair is produced in the high-field region of the device depletion layer by impact ionization. The transit of carriers through the depletion layer leads to generation of microwaves and millimeter waves when the device is tuned in a microwave or millimeter wave cavity. The vast frequency range and high-power output should make the IMPATT a highly suitable device to meet the ever increasing communication needs of the world. IMPATTs have been used in microwave and millimeter wave digital and analog communication systems and in Radars, missile-seekers for defence systems. Si IMPATT diode is designed on the basis of a generalized computer method for DC and current profiles in IMPATT devices starting from the field maximum in the depletion layer. The field-maximum method is suitable for any arbitrary doping profile and involves the determination of the location and magnitude of the maximum field position. In earlier methods, the basic equations (Poisson's and combined current continuity equations) were solved numerically starting from one edge of the depletion layer. The consideration of field maximum position at the edge of the depletion layer may lead to numerical instability. The present method, on the other hand, leads to quick solution of the boundary condition and is especially suitable for design of millimeter wave IMPATT diodes operating at high bias current density, where mobile space charge effect is very large.

Low atmospheric attenuation and high penetrating power of MM-wave signals through cloud, dust and fog at atmospheric window frequencies have made MM-wave communication systems very attractive. In the MM-wave frequency band, 94 GHz is one of the important atmospheric window frequencies around which research activities in the field of MM-wave communication and RADAR systems are centered. In recent time, Wide Band Gap (WBG) semiconductors have proposed as alternative for conventional Si and GaAs, for developing high-power IMPATTs. A few experimental works have been carried out in recent years to explore the possibilities of WBG IMPATTs, especially SiC as base semiconductor material. But the power-level, as obtained from those experiments are much lower than that expected from simulation point of view. This may be due to the lack of maturity of fabrication process technology and complexity in ohmic-contact technology. On the other hand, Si technology is well matured. In order to support ongoing experiments, the authors in this paper have proposed a new optimized design which is carried out through a modified simulation method that includes the realistic doping profile, considering the multi-epitaxial epi-layer growth through MBE. In addition to this, field and temperature dependent electric-field and material parameters of Si are incorporated in the present study to make it more realistic. The present analysis is quite general and it includes mobile-space charge as well as elevated temperature effects. As the diode heats up during the pulse the junction-temperature as well as the device impedance changes accordingly. This study will highlight the important changes in RF-characteristics of the device within a complete pulse. The frequency variation of the device, which is due to the thermal effects, i.e. frequency chirp-bandwidth is obtained from the study. During this study, the authors have varied the device junction temperature within a wide range of 300K - 600K.

Parasitic resistance limits the high-frequency operation of IMPATT devices. Within the pulse duration, due to the increasing junction temperature, the variation of parasitic resistance and power output are estimated through a newly developed simulation technique. For the first time in this paper, the authors have estimated the temperature dependence of the diode admittance that is characterized by two temperatures coefficients.

The effective performance of the device critically depends on the design parameters. Thus authors have made an attempt to study the sensitivity of all the design parameters on the expected power output and efficiency. To the best of

authors' knowledge, this is the first report on sensitivity-modeling of the device.

The present design-optimization study will act as a guide for device engineers to fabricate high-power pulsed mode Si IMPATT, which may be used in tracking RADAR or in any other communication systems.

II. SIMULATION METHODOLOGY

The IMPATT diode is basically a p-n junction diode that operates when it is reverse-biased to avalanche breakdown condition. A one-dimensional model of the p-n junction has been considered in the present analysis. The following are the consideration in the simulation of DC and small-signal behaviour of Si DDR IMPATT diode: (i) the electron and hole velocities have been taken to be saturated and independent of the electric field throughout the space-charge layer, (ii) the effect of carrier space-charge has been considered, (iii) Drift/Diffusion model is considered, (iv) parasitic effects including skin-effect are incorporated in the modelling, (v) realistic doping profile as obtained from the MBE growth is taken into account, (vi) temperature dependent material parameters are taken into account, (vii) asymmetrical structure is considered for analysis.

DC Analysis

The DC-method, described in details elsewhere [Roy (1985), Mukherjee (2008)], considers a generalized (n^{++} n p p^{++}) structure. Here, n^{++} and p^{++} are highly doped substrates and n and p are epilayers. Summarily, in the dc method, the computation starts from the field maximum near the metallurgical junction. The distribution of dc electric field and carrier currents in the depletion layer are obtained by a double-iterative simulation method, which involves iteration over the magnitude of field maximum (E_m), and its location in the depletion layer. The method is used for a simultaneous solution of Poisson and carrier continuity equations at each point in the depletion layer. The field boundary conditions are given by,

$$E(-x_1) = 0 \text{ and } E(+x_2) = 0 \quad (1)$$

Here $-x_1$ and x_2 represent the edges of the depletion layer in n and p regions, respectively.

The boundary conditions for normalized current density P(x), are given by,

$$P(-x_1) = (2/M_p - 1) \text{ and } P(x_2) = (1 - 2/M_n) \quad (2)$$

$M_n = J/J_{ns}$, $M_p = J/J_{ps}$ where J_{ns} and J_{ps} are electron and hole leakage current densities, respectively.

M_p and M_n are hole and electron current multiplication factors, respectively.

$P = (J_p - J_n)/J$, where J_p =hole current density, J_n = electron current density and J = total current density.

Thus the dc field and carrier current profiles are obtained by solving Poisson and carrier continuity equations, when boundary conditions (1) and (2) are satisfied .The realistic field dependence of electron and hole ionization rates, carrier mobility, and the saturated drift velocities of electron ($v_{s,n}$) and hole ($v_{s,p}$) are used in the computation for the profiles of electric field and carrier currents [www.ioffe.ru/SVA/NSM/Semicond/Si.].

The DC to MM-wave conversion efficiency (η) [Gummel (1967)] is calculated from the approximate formula,

$$\eta\,(\%) = (V_D \times 100)/(\pi \times V_B) \quad (3)$$

where, V_D = voltage drop across the drift region . Also, $V_D = V_B - V_A$, where, V_A = voltage drop across the avalanche region, and, V_B = breakdown voltage.

Avalanche breakdown occurs in the junction when the electric field is large enough such that the charge multiplication factors (M_n, M_p) become infinite. The breakdown voltage is calculated by integrating the spatial field profile over the total depletion layer width, i.e.,

$$V_B = \int_{-x_1}^{x_2} E(x)dx \quad (4)$$

where, $-x_1$ = n-side depletion layer width and, $+x_2$ = p-side depletion layer width

Small Signal Analysis

The small signal analysis of the IMPATT diode provides insight into the high frequency performance of the diode. The range of frequencies exhibiting negative conductance of the diode can easily be computed by Gummel-Blue method [Gummel (1967)]. From the dc field and current profiles, the spatially dependent ionization rates that appear in the Gummel-Blue equations are evaluated, and fed as input data for the small signal analysis. The edges of the depletion layer of the diode, which are fixed by the dc analysis, are taken as the starting and end points for the small signal analysis. On splitting the diode impedance Z (x,ω) obtained from Gummel–Blue method, into its real part R (x,ω) and imaginary part X (x,ω), two differential equations are framed [Mukherjee (2008)]. A double-iterative simulation scheme incorporating modified Runge-Kutta method is used to solve these two equations simultaneously. The small signal integrated parameters like negative conductance (-G), susceptance (B), impedance (Z), frequency band width, and the quality factor (Q) of the diode are obtained satisfying the boundary conditions derived elsewhere [Mukherjee (2008)].

The simulation method provides the high-frequency negative resistance and negative reactance profiles in the space-charge layer of the device. The diode negative resistance ($-Z_R$) and reactance ($-Z_x$) are computed through numerical integration of the -R (x) and -X (x) profiles over the active space-charge layer.

Thus,

$$-Z_R = \int_{-x_1}^{x_2} -R\,dx \quad \text{and} \quad -Z_X = \int_{-x_1}^{x_2} -X\,dx$$

The diode impedance Z is given by,

$$Z(\omega) = \int_{-x_1}^{x_2} Z(x,\omega)\,dx = -Z_R + jZ_X \quad (5)$$

The diode admittance is expressed as,

$Y = Z^{-1} = -G + jB = (-Z_R + j Z_X)^{-1}$

or, $-G = -Z_R/((Z_R)^2 + (Z_X)^2)$ and

$$B = Z_X/((Z_R)^2 + (Z_X)^2) \quad (6)$$

It may be noted that both –G and B are normalized to the area of the diode.

The small-signal quality factor (Q) is defined as the ratio of the imaginary part of the admittance to the real part of the admittance (at the peak frequency), i.e.,

$-Q_p = (B_p/-G_p)$

At a given bias current density, the peak frequency (f_p) is the frequency at which the negative conductance of the diode is a maximum, and the quality factor is a minimum.

At resonance, the maximum RF power output (P_{RF}) from the device is obtained from the expression [Mains (1983):

$$P_{RF} = (V_{RF}^2 . G_P . A)/2, \quad (7)$$

where V_{RF} (amplitude of the RF swing) is taken as $V_B/2$, assuming a 50% modulation of the breakdown voltage V_B and A is the area of the diode. The diode negative

conductance at the optimum frequency ($-G_p$) is normalized to the area of the diode. The role of parasitic positive series resistance [Adlerstein (1983)] is also considered for calculating realistic values of P_{RF}.

III. RESULTS AND DISCUSSIONS

Table 1: Si IMPATT diode at W-band: Different active layer width and doping concentration.

SET 1	SET 2	SET 3	SET 4
Wn=0.30µm Wp=0.28µm $N_A=1.8x10^{23}m^{-3}$ $N_D=2.0x10^{23}m^{-3}$ $N_H=1x10^{26}m^{-3}$	Wn=0.35µm Wp=0.32µm $N_A=1.6x10^{23}m^{-3}$ $N_D=2.0x10^{23}m^{-3}$ $N_H=1x10^{26}m^{-3}$	Wn=0.37µm Wp=0.34µm $N_A=1.4x10^{23}m^{-3}$ $N_D=1.8x10^{23}m^{-3}$ $N_H=1x10^{26}m^{-3}$	Wn=0.35µm Wp=0.30µm $N_A=1.8x10^{23}m^{-3}$ $N_D=2.3x10^{23}m^{-3}$ $N_H=1x10^{26}m^{-3}$

Table 2: Si IMPATT diode at W-band: Different design analysis

Design Data	SET 1	SET 2	SET 3	SET 4
Operating Current(A)	8.0	7.5	7.5	8.5
Maximun Electric Field ($10^7 V/m^{-1}$)	6.5	6.2	6.3	6.3 0
Breakdown Voltage(V)	22.5	22.0	21.5	20.0
Efficiency(%)	9.7	9.5	10.6	9.
Peak Output Power(W)	18.0	19.3	20.2	20.7
Peak negative conductance(10^6 Sm^{-2})	38.0	35.5	42.5	46.0
Parasitic resistance including skin depth (Ω)	0.24	0.32	0.37	0.30
Diode negative resistance (Ω)	1.1	0.97	1.1	1.0
Avalanche frequency (GHz)	80.0	78.0	85.0	86.0
Peak frequency (GHz)	85.0	94.5	98.5	101.0
Quality factor	1.2	1.42	1.05	1.1

Optimisation of pulsed DDR IMPATT

Table 1 shows the design parameters of the diodes. Four sets of design parameters are considered in this paper to choose the optimum diode. To achieve this goal, the depletion region width, current, background doping concentration of the diodes are varied accordingly. Since the main objective of the design is that the device should operate in pulsed mode, it is note worthy to menion that the operating current should be much higher than that in CW mode. So the effects of increasing bias current on the peak frequency, efficieny and adittance charecteristics are studied and ploted in Figures 1 and 2. From Figure 1, it is cear that with the increasing current (from 5 A to 10 A) the peak frequency, in case of Set I diode increase from 85 GHz to 110 GHz, Set 2 diode increase from 87 GHz to 108 GHz, Set III diode increases from 90 GHz to 104 GHz and Set 4 diode increases from 87 GHz to 109 GHz. Thus in case of Set III diode, the upshift of frequency with bias current is quite moderate, compared to other three sets.

If we consider the effects of increasing bias current on the efficiency of the devices, it is interesting to observe that effcecy in case of Set 1 and Set II devices decrease to almost 6% at a high bias current ~10 A, but the effciency in Set III and set IV diode remain at around 9% at a current of 10 A. This may be due to the fact that mobile space charge effect becomes prominent in Set I and Set II diodes at a current above 10 A, while the same is quite moderate in Set III and Set IV devices even at a current of 10A.

The admittance charecteristics of all the 4 sets of diodes are compared and shown in Figure 2. Quality factor and negative reistance are found to be better in Set III device. Thus the authors have considered the Set III diode for further analysis in this paper.

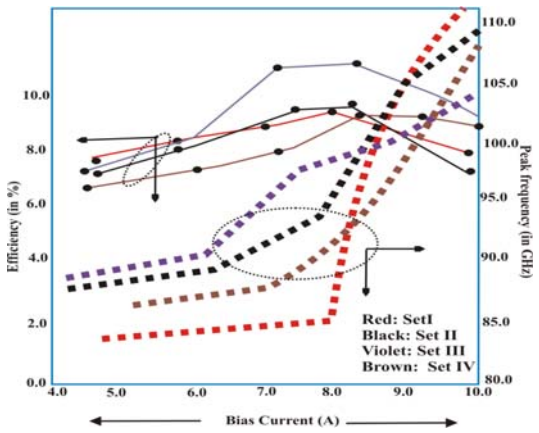

Figure 1: Bias current optimization of the designed diode at W-band

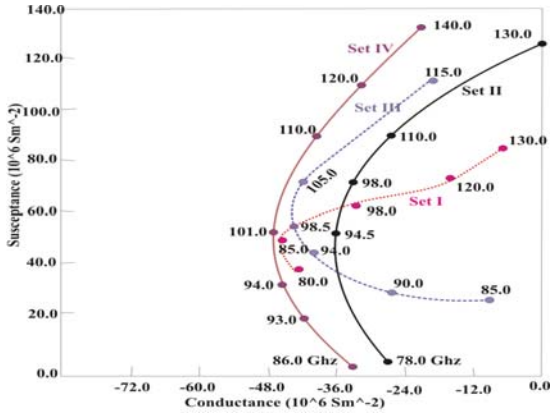

Figure 2: Admittance plots of the designed diodes

IV. SENSITIVITY ANALYSIS

To make an optimum design, the effects of modifying depletion layer width, doping concentration, current density and junction temperature on the device performance is studied. In this study the quantitative and qualitative variation of performance of the device as a result of variation of input of the model is studied. In more specifically, sensitivity analysis investigate the robustness of a study when the study includes some form of mathematical modelling. In order to optimize the device performance, the authors have investigated the effect on power output and frequency of the device due to the variation of the critical design parameters. 'Sensitivity analysis' as presented in this modelling is four-fold, i.e. (a) temperature sensitivity (b) Depletion layer width sensitivity, (c) background doping concentration sensitivity.

Temperature Sensitivity (design based on Set III diode)

Since the thermal conductivity of Si is low and the design deals with the high-current operation, the authors have studied the performance of the diode at a high-junction temperature, 500K. Baed on that modeling, the authrs have futher studied the effect of increasing or decreasing lattice temperature on the (i) Peak frequency, (ii) Negative conductance, (iii) Negative resistance and (iv) Positive resistance of the device. The temperature dependence is shown in Figures 3 and 4. It is found that within the

temperature range 460K-520K, the device performance , as far as the above-mentioned diode parameters are conerned, degrade moderately, by 4% (device negative conductance), 35% (negative resistance) and 16% (diode negative resistance). Since the degradation of device negative resistance and increase of parasitic resistance are quite serious abve 550K, it is better to restrict the juncion and/or lattice teperature below 550K. Table-2 shows the effect of temperature on various diode parameters. It is found that due to the variation of junction emperature from 450K – 550 K, quality factor degrades seriously, by 70% and power output, P_{max} decrease by 25%. In Figures 3 and 4, the authors have indicated an operating zone, which indicates comparatively less temperature sensitive zone, where the practical device could operate.

Table 2: Temperature sensitivity of Set III diode

Temperature (K)	E_{max} (10^7 V/m)	V_B (V)	$-Q_P$	η (%)	P_{max} (W)
300.0	5.72	18.2	0.75	11.7	27.0
350.0	5.85	18.2	0.82	11.4	25.0
400.0	6.0	18.4	0.95	11.0	23.3
450.0	6.2	19.7	1.0	10.8	20.8
500.0	6.25	20.2	1.1	10.6	20.7
550.0	6.37	21.6	1.7	7.5	15.6

Depletion layer width Sensitivity (design based on Set III diode): The active region width, both in n-side and p-side are varied to determine the sensitivity of the design. The effects are shown in Figures 4 and 5. Depletion region width in the n-side is varied from 0.3μm to 0.42μm. The effects of this variation on peak frequency and negative conductance are shown in Figure 5. It is found that with the increasing n-region width from 0.3μm to 0.42μm, peak frequency decrease from 113 GHz to 95 GHz. Negative conductance initially increase from $38x10^6$ $S.m^2$ to $43.0x10^6$ $S.m^2$. But when the width increase beyond 0.4μm, negative conductance degrades seriously, as shown in the figure. This may be due to the fact that with the increasing width (keeping other parameters unaltered), un-depleted region width increases and that increases series resistance (table 3) and this in turn decrease negative conductance and power output. With the increasing active region width from 0.35μm to 0.37μm, i.e. 6%, it is observed that the peak frequency decrease by 2.5%, negative conductance as well as power output decrease by 4%. The effects of increasing n-region width on the other paramters are shown in Table 3. It is depicted from Table 3 that 5% alteration of n-layer width, changes quality factor by 20% and changes P_{max} by 25%.

In the similar way, the depletion region-width in the n-side is varied from 0.27μm to 0.39μm. The effects of this variation on peak-frequency and negative-conductance are shown in Figure 6. It is found that with the increasing p-region width from 0.27μm to 0.39μm, peak frequency decrease from 113 GHz to 93.0 GHz. Negative conductance initially increase from $38x10^6$ $S.m^2$ to $42.5x10^6$ $S.m^2$. But when the width increase beyond 0.35μm, negative conductance degrades seriously, as shown in the figure. This may be due to the fact that with the increasing width (keeping other parameters unaltered), un-depleted region width increases and that increases series resistance (table 4,) and this in turn decrease negative conductance and power output. With the increasing active region width from 0.32μm to 0.35μm, i.e. 6%, it is observed that peak frequency decrease by 2.0%, negative conductance as well as power output decrease by 6%. The effects of increasing p-region width on the other paramters are shown in Table 4. It is depicted from Table 4 that 5% variation of p-layer width changes quality factor by 9% and P_{max} by 12.5%.

Thus it is observed that the device is more sensitive for alteration in p-width, whereas less sensitive for alteration in n-width.

Table 3: Depletion layer width (n-side) sensitivity of SET III diode

Active region width (n-side) (μm)	E_{max} (10^7 V/m)	V_B (V)	$-Q_P$	R_s (Ω)	P_{max} (without R_S) (W)
0.34	6.45	19.0	0.75	0.30	18.0
0.35	6.42	18.4	0.82	0.35	17.3
0.36	6.32	19.0	0.95	0.35	18.3
0.37	6.30	21.5	1.05	0.37	24.0
0.42	633	21.0	1.76	0.64	20.0

Table 4: Depletion layer width (p-side) sensitivity of SET III diode

Active region width (n-side) (μm)	E_{max} (10^7 V/m)	V_B (V)	$-Q_P$	R_s (Ω)	P_{max} (without R_S) (W)
0.32	6.42	20.0	0.92	0.32	20.0
0.33	6.40	20.8	1.14	0.35	21.0
0.34	6.30	21.5	1.05	0.37	24.0
0.35	6.32	21.5	1.20	0.45	21.7
0.39	6.33	21.2	1.23	0.56	17.6

Background Doping Sensitivity (design based on Set III diode): Background doping concentration, both in n-side and p-side is varied to study the doping sensitivity. N_D is varied from $1.2x10^{23}$ to $1.8x10^{23}$ m^{-3}. The variation is showin Figure 7. In the low doping region, due to the heavily punch-through condition, negative conductance, negative resistance, power are reasonably low, however, with the decreasing punch-through, i.e. with the increasing doping concentration, negative conductance, negative resistance and power output improves gradually as shown in Figure 7 and Table 5. With the 10% decrease of N_D from $1.4x10^{23}$ m^{-3}(SET III) , Q_P and P_{max} degrade by 3 times and 66%, whereas, 10% increase of N_D from the same value decrease Q_P and P_{max} by 1.2 times and 1.5%.

Dependence of variation of accepter doping concentration, N_A is shown in Table 6. The corresponding variation is shown in Figure 8. Table 6 shows the variation of diode parameters with N_A. The nature of variation of negative conductance with N_A , as shown in Figure 8, is similar to that of Figure 7, only with the difference in magnitude. This simulation experiment indicate that the 10% reduction of N_A from $1.8x10^{23}$ m^{-3} (SET III) degrade Q_P and P_{max} by 3 times and 60%, respectively, whereas, 10% increase of N_A from the said value (SET III) degrade Q_P and P_{max} by 1.3 times and 1.3%, respectively.

Thus it is observed that the increasing N_D and N_A has less pronounced effect on the device performace than that of decreasing N_D.

Table 5: Doping (n-side, N_D) sensitivity of SET III diode

Background doping (n-side)(10^{23} m^{-3})	$-Q_P$	$R_S(\Omega)$	P_{max}(W)
1.2	3.5	0.87	8.0
1.3	2.3	0.82	11.0
1.4	1.05	0.37	24.0
1.5	1.1	0.35	23.4
1.6	1.25	0.33	23.7
1.7	1.7	0.32	22.3

Table 6: Doping (p-side, NA) sensitivity of SET III diode

Background doping (n-side) (10^{23} m^{-3})	$-Q_P$	$R_S(\Omega)$	P_{max}(W)
1.6	3.1	0.81	9.5
1.7	2.3	0.82	12.3
1.8	1.05	0.37	24.0
1.9	1.13	0.35	23.6
2.0	1.32	0.37	23.7
2.1	1.30	0.36	22.0

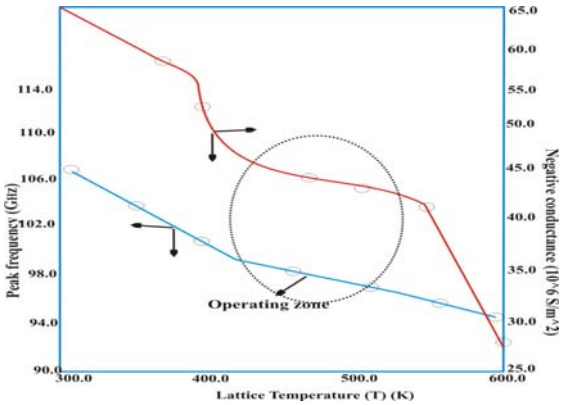

Figure 3: Temperature effects on RF properties of Si DDR IMPATT at W-band.

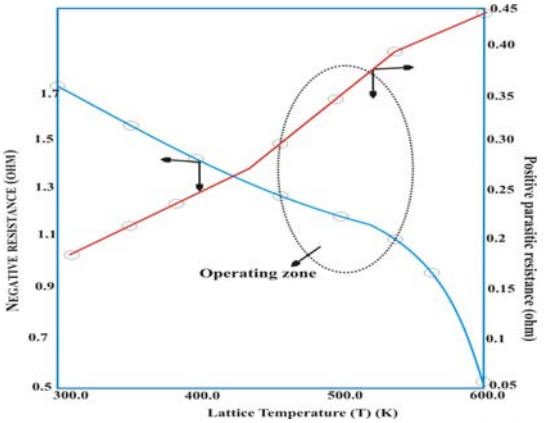

Figure 4: Temperature effects on Si DDR IMPATT at W-band

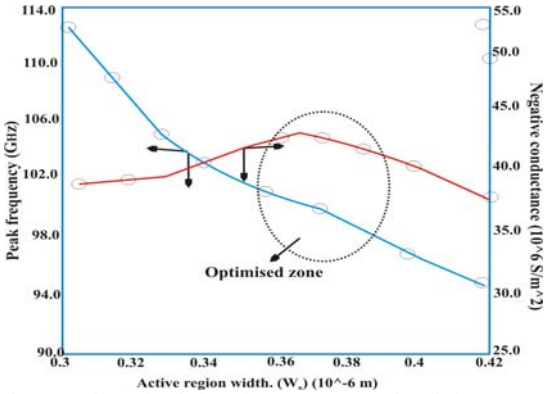

Figure 5: Effect of variation of W_n on RF properties of Si IMPATT

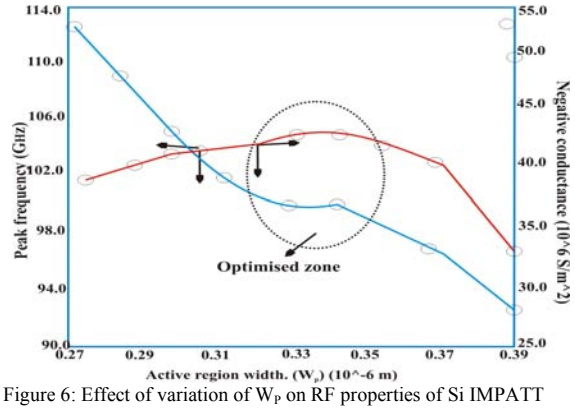

Figure 6: Effect of variation of W_P on RF properties of Si IMPATT

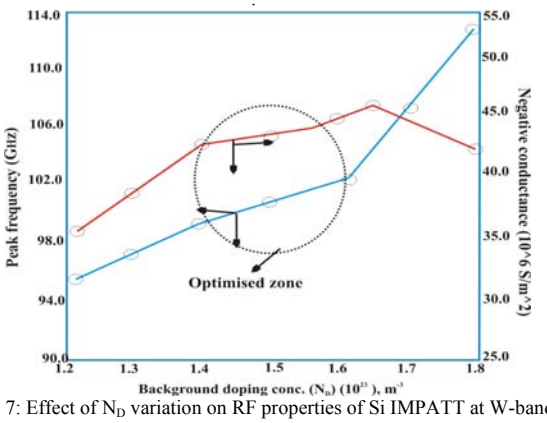

Figure 7: Effect of N_D variation on RF properties of Si IMPATT at W-band.

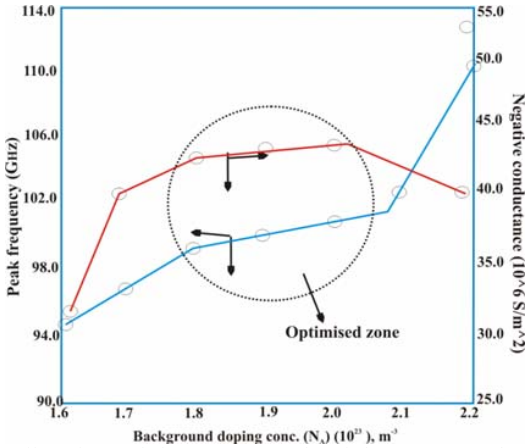

Figure 8: Effect of N_A variation on RF properties of Si IMPATT at W-band.

V. CONCLUSIONS

Si based IMPATT diode at W-band is optimized for generation of RF power of ~20W. The effects of parasitic resistance, elevated temperature are incorporated in the analysis.

The IMPATT diode has been analyzed primarily from the point of view of device characteristics in the limit of small RF signals (20% modulation). This generalized small-signal analyses have provided a considerable insight into the device-operation. To the best of authors' knowledge this is the first study on the details sensitivity modelling of the pulsed IMPATT diode. This detail modelling will help device engineers to fabricate optimized high-power pulsed IMPATT diode.

ACKNOWLEDGEMENT

The authors wish to acknowledge Director,CMSDS for his keen interest in this work.

REFERENCES

1. Adlerstein M.G., Holway L.H., Chu S.L., Measurement of series resistance in IMPATT diodes, IEEE Trans. Electron Devices, vol. ED-30, p. 179,1983.
2. Electronic Archive: New Semiconductor Materials, Characteristics and Properties (Online) www.ioffe.ru/SVA/NSM/Semicond/Si.
3. Gummel H. K, Blue J. L., A small signal theory of avalanche noise in IMPATT Diodes", IEEE Trans. Electron Devices, vol. 14, p. 569, 1967.
4. Mains R. K. and Haddad G. I, Properties and capabilities of millimeter wave IMPATT diodes, Infrared and Millimeter Waves, vol. 10, Book chapter 3, pp. 124-125,1983.
5. Mukherjee M., Mazumder N. and Roy S. K., GaN IMPATT diode: A photo-sensitive high-power Terahertz source", Semiconductor Sc and Technology, vol. 22, p. 1258, 2007.
6. Roy S K, Banerjee J P and Pati S P, A Computer analysis of the distribution of high frequency negative resistance in the depletion layer of IMPATT Diodes", *Proc.4th Conf. on Num. Anal. of Semiconductor Devices (NASECODE IV) (Dublin) (Dublin: Boole),* pp. 494-500,1985.