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Modeling a MOSFET for Monolithic Millimeter-wave Integrated Circuit Design

Adhira Raj, Karthigha Balamurugan, Jayakumar M

Amrita Vishwa Vidyapeetham,Coimbatore,India,

***Abstract*— The millimetre-wave spectrum at 30-300 GHz is of increasing interest to service providers and systems designers because of the wide bandwidths available for carrying communications at this frequency range. These wide bandwidths are valuable in supporting applications such as high speed data transmission and video distribution. This project mainly focuses on modeling a MOSFET for millimeter-wave integrated circuits(MMIC). There are many emerging millimeter-wave applications which demand for low unit cost manufacturing solutions. With the advent of millimeter-wave semiconductor technology a MOSFET is modeled to work efficiently at high frequency. The transistor modeling is done by developing a compact model with BSIM3v3 and external parasitics to model substrate and gate resistance. High frequency MOSFET compact model built using BSIM3v3 as intrinsic core and having parasitic elements supporting HF are designed as extrinsic subcircuit. To demonstrate the effectiveness of the proposed composite MOSFET model, the proposed methodology is then used in designing a low power millimeter-wave CMOS low noise amplifier. S-parameter analysis is to be verified for non linear large signal transistor model analysis of millimeter-wave signals. A hybrid millimeter-wave modeling is done using ansoft designer by designing the appropriate extrinsic region.**

***Keywords*— Monolithic millimetre-wave integrated circuit (MMIC), CMOS millimeter-wave integrated circuits, LNA-low noise amplifier, high frequency (HF) behaviour, composite model, Bsim3v3.**

I. INTRODUCTION

There is rapid growth in mobile telecommunication market leading to new technology developments in the analog integrated circuit design at high frequencies. The Radio frequency integrated circuits (RFIC's) based on CMOS processes are of high demand due to the low cost, low-power characteristics of CMOS technology, availability of passive components, and possibilities for System-on-Chip (SoC) integration. Thus CMOS circuit integration is found to be highly feasible in RF application.

The high-speed and broadband wireless data transmission is required due to the increase in demand for high-performance personal computers (PCs) and multimedia equipment in offices and homes. This requirement makes wireless indoor communication systems such as wireless local area networks (WLAN) and personal area networks (PAN) more prominent. The millimeter-waves are found to be more significant for transmission in the case of short-range indoor broadband WLAN and PAN systems. The microwave frequency bands have been saturated and thus there is growing need to exploit new frequency bands which could supply enough bandwidth for transmission of multimedia content. For this reason, utilization of the millimetre-wave band has been recommended, and developing millimetre-wave wireless LAN in recent years. It is found that there has been an increasing requirement for the development of the V-band WLAN for commercial applications [1]. Advantages of millimetre-wave communication are very wide frequency band, high-speed transmission, and radiated power limitation for unlicensed use.

II. MILLIMETER-WAVE TECHNOLOGY

The millimeter-wave band frequency ranges from 30-300GHz allowing huge frequency allocations. The 60GHz band provides 7GHz of unlicensed spectrum. The worldwide availability of 7GHz unlicensed band around 60GHz is a real opportunity for development for next generation Wireless Personal Area networks(WPANs). Personal Area Networks or short distance wireless networks, WPANs address wireless networking of portable and mobile computing devices. The millimeter-wave band provides point to multipoint access with multi Gbps throughput. The frequency of 60 GHz is very useful for short-distance wireless communications due to the strong absorption characteristic by oxygen in the atmosphere. This improves the frequency efficiency when compared to other frequency bands. millimeter-wave band is suitable for wireless networks due to the presence of higher speed transmission, exploitation of antenna directivity, simple modulation and demodulation and simple signal processing.

III. HIGH FREQUENCY SOLID STATE DEVICE PERFORMANCE

The IC design is heavily dependent on the accurate device models based on circuit simulation as fabrication is highly expensive. There is very high development found in the silicon integrated circuit operating at high frequency. There are many works done in modifying the channel length and gate width parameters that would intern effect the working of MOSFET.

Compact models are interface between technology and the design. The physical 3D numerical models of the semiconductors included the drawback of having very high computational time simulation. Thus experimenting with compact models is expensive and time consuming. The compact models comprises of a combination of physical and empirical methods. The parameter equations are developed describing the behaviour of this compact model. Several compact models are found for digital and analog. The compact model they are found to be inaccurate when working at high frequency as it does not take into account the geometry-dependent couplings. Lots of work [3] have been done in recent years where various authors have emphasized in amending the available MOS transistor model. At millimetre wave frequency, MOSFET has parasitic capacitances and resistances which have to be considered while designing millimetre wave circuit.

A. *Generation of MOSFET models*

The selection of the MOSFET model type for use in analysis usually depends on the electrical parameters critical to the application. There are different generations of MOS models:

The Generation I MOS model which is based on the equivalent model. The parasitic elements are derived by parametric extraction method for particular frequency range. This includes the LEVEL 2 models considering the bulk charge effects on current. This model accounts velocity saturation, mobility degradation and DIBL. The Generation II model mainly concentrates on mathematical modeling. There is less focus on developing exact analytical models. The process of modifying the model parameters for different values of drawn channel length and width was done. This Generation II includes the BSIM models consider's the variation of model parameters as a function of sensitivity of the geometric parameters. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects. The Generation III is the model that was developed for higher frequency range operations. Here enhanced version of I_{ds} equation from LEVEL 2 model was developed. There is variation from LEVEL 2 model found in terms of area regarding Substrate doping, Threshold voltage, Effective mobility, Channel length modulation and Sub-threshold current. The EKV3.0 compact MOS transistor model integrates many years of research & development from several university teams in Europe. The EKV3.0 model addresses needs of advanced analog/RF design using most advanced CMOS technologies including the sub-0.1um era. This model supports the efficient working of analog circuitry and RF CMOS, due to the presence of ideal charge-based model along with scalable model for short and narrow channel devices.

IV. CMOS TECHNOLOGY

The incredible growth in CMOS market has caused the rapid development of CMOS technology that lead to the advancement of linear devices. The mobile telecommunication market emphasizes the need for reliable analog integrated circuit design at high frequencies. The rapid scaling of CMOS to shorter channel lengths has enabled the circuits to operate at millimetre-wave frequency range. The three-dimensional parameters are more difficult to control thus CMOS technology leads to better controlled process with less variation in crucial device parameters. CMOS technology proves to endow all these features [13] in analog and digital IC design.

The major advantages of silicon gate CMOS compared to metal gate linear ICs are their higher speed and lower power consumption. These features impact a broad range of device performance parameter. A faster chip widens the scope of possible applications and increases signal quality and reliability. For a given frequency response, power can be reduced. The CMOS ICs can respond to higher frequency inputs, the timers can oscillate at higher frequencies, and the response times of operational amplifiers and comparators are reduced while slew rate and operating frequency increase. All of these qualities give wider signal frequency range and operating and providing increased accuracy and gain bandwidth at reduced voltages and power requirement over broad operating conditions. The low power consumptions of CMOS linear chips is advantageous in a number of different ways. This lessens the dependence of timing accuracy on expensive components, increasing the accuracy and reducing the cost of the timing function. In addition, as the number of transistors per chip increases, the low power consumption of CMOS ICs allow greater densities but will require little or no external cooling and very little self-heating design considerations.

In the MOSFET modeling parameter consideration to fabricate the devices for the 60-GHz wireless LAN system, the development of active devices that have a high frequency, low noise, and high power performance is an essential criteria. Semiconductor technology is the only solution to make these applications achieved in real time. Also CMOS implementation promises higher level of integration, low cost and low power consumption.

Designing of MOS model at high frequency is more challenging because as the operating frequency increases to gigahertz range. The parasitic components play a very important role and hence they are to be designed such that less parasitic components used in real time giving higher gain. So the proposed model should predict these components accurately at HF and also the requirements of MOSFET model in low-frequency application such as continuity, accuracy and scalability of the dc and capacitance models should be maintained.

B. *MOSFET modeling issues*

The study of high frequency MOSFET started with the development in technology. One of the oldest study on the MOSFET behaviour at high frequency was done by Y. Tsividis [11]. The work done by Y. Tsividis is general and theoretical discussing the behaviour by different equivalent circuits, considering both quasi-static and non-quasi-static operations. The parasitic resistance was not considered in the early ages. The beginning of 1990s the MOSFET models were designed by considering the effect of parasitic gate resistance[12] as it was a very crucial RF component. There were many studies done on modeling of RF CMOS and after facing lot of challenges achieved a scalable model accurate in all regions of operation at high frequency. The modifications were done on the extrinsic gate resistor focusing on the output impedance modeling with substrate resistance network. At low frequencies the drain conductance nonlinearity was an important factor but for high frequencies the capacitance effect lead to a dominant nonlinearity source by the transconductance. Even with the newer models like BSIM3 and BSIM4, nonlinearity is a problem at zero-drain voltage [13].

1) *Small signal equivalent circuit for MOSFET*: When the equivalent circuit is linearized with quasi-static approximation we get the small signal equivalent circuit. The model consists of current model, active charges, parasitic capacitances and parasitic series resistances. The first proposed equivalent circuit [15] suitable for high frequency applications used in this is based on the original SPICE equivalent circuit for the MOSFET. The Fig.3. depicts the modified equivalent circuit with the added improvement under the substrate short-circuited to source condition. The

new elements added to this equivalent circuit include Rgs, Rgd, Rdb, Cds, and Lg.

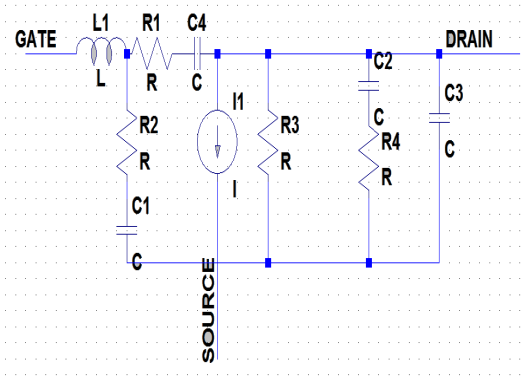

Fig. 1 Broadband small-signal equivalent circuit Of the MOSFET used for wave simulation.

2) BSIM3v3 RF Model: With the advent of submicron technologies, GHz RF circuits can now be realized in a standard CMOS process. This method becomes prohibitively complex when used to simulate highly integrated CMOS communication systems. Hence, a compact model, valid for a broad range of bias conditions and operating frequencies is desirable. BSIM3v3 has been widely accepted as a standard CMOS model for low frequency applications.

The new BSIM3v3 RF model is realized with the addition of three resistors Rg, Rsubd, and Rsubs to the existing BSIM3v3.1 model. Rg, models both the physical gate resistance as well as the non-quasi-static (NQS) effect. Rsubd and Rsubs are the lumped substrate resistances between the source/drain junctions and the substrate contacts. The values of Rsubd and Rsubs may not be equal as they are functions of the transistor layout. To demonstrate the accuracy of the model the s-parameter analysis is done.

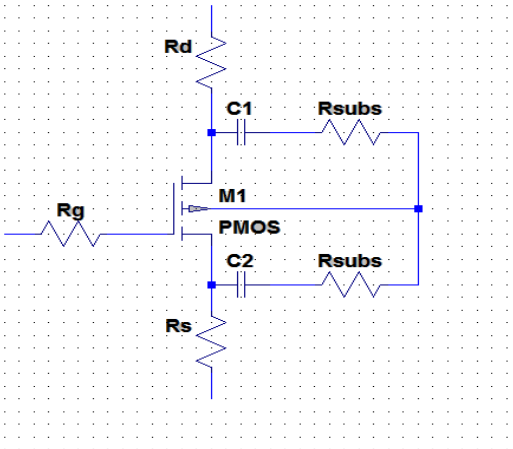

Fig.2. A basic MOSFET HF model built on BSIM3v3

An accurate scalable small-signal RF CMOS model applicable to high frequencies is developed using parasitic elements is discussed. Due to multimetal layers, vertical interconnects, substrate loss and substratecontact rings, the extrinsic parasitic network of CMOS field-effect transistor (FET) is more complicated than GaAs FETs and does not follow simple scaling rules. In this work [18], we have employed 3-D EM simulation to derive the scaling rules of theCMOSFETs. The de-embedding technique is used to verify the effects of pads and interconnects. A complete scalable RF CMOS model is constructed by combining the scalable extrinsic network with the intrinsic CMOS network. A general field-effect transistor (FET) device model is composed of the intrinsic and extrinsic networks. Intrinsic device model is comprised of bias-dependent elements which can be modeled by lumped elements. It is well known that intrinsic parameters are linearly scalable with the total gate periphery of the device. The extrinsic network is bias independent and depends primarily on the physical layout of the devices such as the interconnects, electrode structures and probe pads.

V. MILLIMETER-WAVE MOSFET MODELING

A compact model, valid for a broad range of bias conditions and operating frequencies is desirable. BSIM3v3 has been widely accepted as a standard CMOS model for low frequency applications.

A. *AC small-signal modeling*

In this, the four-terminal MOSFET can be divided into two portions: intrinsic part and extrinsic part. The concepts of equivalent circuits representing both intrinsic and extrinsic components in a MOSFET are analyzed to obtain a physics-based RF model. The intrinsic part is the core of the device without including parasitic components. The extrinsic part consists of all the parasitic components. These parasitic component, they cannot be avoided in reality, as these components are needed for high-frequency operation.

1) *Modeling of the Intrinsic MOSFET:*

Here implementing based on factors such as normal and reverse short-channel and narrow-width effects, channel length modulation, drain-induced barrier lowering (DIBL), velocity saturation, mobility degradation due to vertical electric field, impact ionization, band-to-band tunnelling, polysilicon depletion, velocity overshoot, self-heating, and channel quantization are considered. Considering the various effects, a BSIM3v3 model as the intrinsic component is selected. BSIM3v3 has been widely accepted as a standard CMOS model. This model is mainly selected as it is found to be more advantageous, as the Drain current could easily be modified by current equation and this model mainly comprises of an accurate capacitance model.

2) *Subcircuit Model:*

As we discussed above, a MOSFET contains many extrinsic components such as gate resistance, source/drain series resistance, substrate resistance and capacitance, and gate overlap capacitance.

The source and drain series resistances have been added outside the MOS model since the internal series resistances are only soft resistances embedded in the expression used to calculate the drain current to account for the dc voltage drop across the source and drain resistances,(but they do not add any poles and are therefore invisible for ac simulation). The substrate resistances have been added to account for the signal coupling through the substrate.

Gate Resistance is known that the gate resistance impacts impedance matching to achieve maximum power transfer and increases the noise figure of the transistor due to the thermal noise introduced by the gate resistance. The gate resistance is in principle a bias-independent component at dc and low

frequency, but may contain the contribution of an additional component with bias dependence at HF.

The effective gate resistance consists of two parts:

$$R_G=R_{Gpoly}+R_{Gnqs} \quad (1)$$

where R_{Gpoly} is the distributed gate electrode resistance from the polysilicon gate material and R_{Gnqs} is the NQS distributed channel resistance seen from the gate and is a function of both biases and geometry.

The parameter $R_{G,poly}$ is determined by

$$R_{G,poly}=(\underline{R_{Gsh}}/ N_f L_f)(W_{ext}+W_f/ \alpha) \quad (2)$$

where $\underline{R_{Gsh}}$ is the gate sheet resistance, W_f is the channel width per finger, L_f is the channel length, N_f is the number of fingers, and W_{ext} is the extension of the polysilicon gate over the active region.

The parameter R_{Gnqs} is determined by i) the static channel resistance (R_{st}), which accounts for the dc channel resistance; ii) the other is the excess diffusion channel resistance (R_{ed}) due to the change of channe1 charge distribution by ac excitation of the gate voltage. R_{st} and R_{ed} together determine the time constant of the non-quasistatic effect.

Fig.6. shows the basic MOSFET model containing resistive elements as their parasitic.

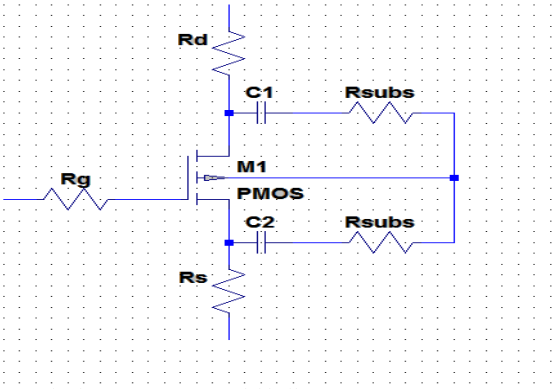

Fig.3. A basic MOSFET HF model built on BSIM3v3.

Drain and Source resistances (without including any bias dependence) can be described by

$$R_D=R_{D0}+r_{dw}/N_f W_f \quad (3)$$

$$R_S=R_{S0}+r_{sw}/N_f W_f \quad (4)$$

where r_{dw} and r_{sw} are the parasitic drain and source resistances with unit width, R_{D0} and R_{S0} account for the part of the series resistances without the width dependence. Using equations (1)-(4), a composite MOSFET model is constructed as in fig.7. In designing the influence of the substrate resistance is ignored.

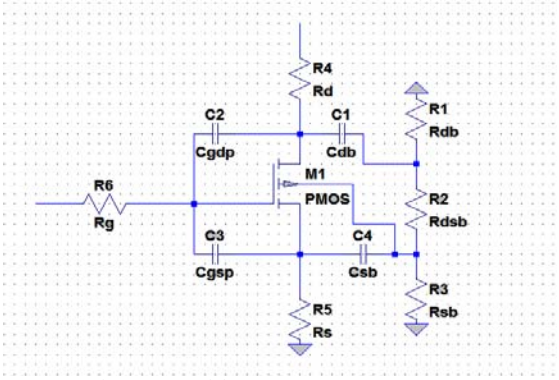

Fig.4. Composite MOS Model

The Capacitance model in the modeling of MOS transistor capacitances has followed one of two distinct approaches: the conventional approach, also known as the gate-capacitance approach. Here the charge-based approach, the MOS transistor is treated as a four-terminal voltage-controlled capacitor. This approach is based on the ability to determine the MOS transistor gate, bulk, source, and drain charges, which are used to derive the transient currents and the capacitances through mathematical differentiation with respect to time and voltage, respectively. Defining charges rather than capacitances as the state variables in the circuit simulator avoids the charge non conservation problem associated with the conventional approach. The substrate capacitance is an extrinsic capacitance that should be included in a subcircuit model for ultra HF (much higher than 10 GHz) applications.

B. *De-embedding*

The device modelled should be verified to work at high frequency applications with high gain. The de-embedding technique is used for this purpose. The de-embedding technique can be classified as modeling based approach and measurement based approach. To get the DUT response from measurement the pad parasitics must be removed an dthe device should be verified. The changing of measurement results for pad parasitic of the DUT is often called pad de-embedding.

1) *Pad de-embedding techniques:*

The main interest in RF probing for device characterization purposes is to characterize the intrinsic device for the purpose of modeling its behavior at the GHz frequencies when embedded in an IC design environment. It is obvious that the intrinsic device in an IC design environment will not have probe pads attached to it except when used as a test structure. Therefore, the probe pad parasitic effect must be de-embedded from the measurement since a measurement on wafer with calibrated probe tips has the intrinsic device characteristics plus pad parasitics. There are two approaches for de-embedding pad parasitics. One approach is to place calibration patterns for standards (open, short, load, through) on the same test die with pads, which also mimic the DUT pads, and use these standard patterns for network analyzer calibration. This approach has the advantage of having calibration standards on the same material, which is silicon for CMOS as DUT.

VI. EXPERIMENTAL RESULTS

A. *Composite model verification*

The composite MOSFET model suitable for high frequency IC is done. The BSIM3v3 is used as the intrinsic part. The extrinsic part is built by lumped elements. Using the composite MOSFET model, a single stage LNA [28] is simulated using circuit simulator MICROCAP-10. This LNA model is shown in Fig.5.

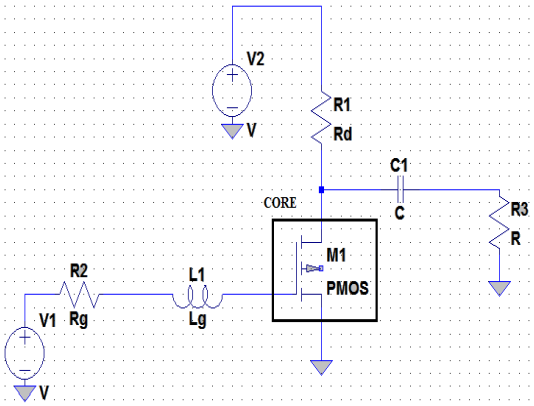

Fig.5. Single stage LNA

The Fig.6. and Fig.7. shows the verification of the developed MOSFET composite model in an amplifier design by comparing with and without composite subcircuit model. Thus in the above figure Fig.8. single stage LNA the simulation is done in Microcap10, this simulation is done by checking the design with and without subcircuit.

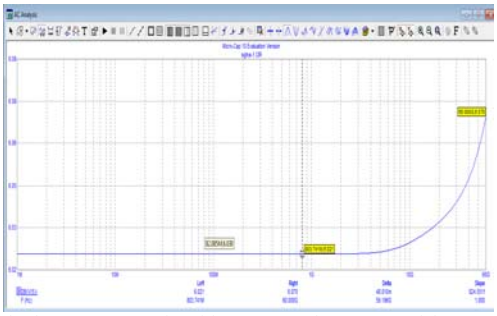

Fig.6.Single stage LNA gain without composite MOS model

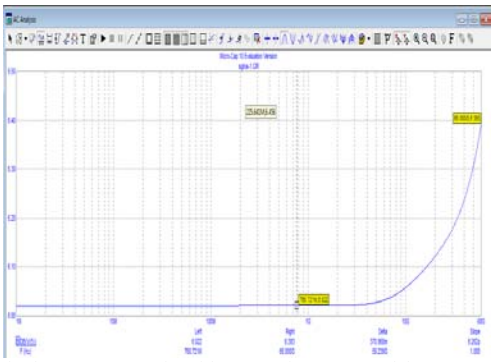

Fig.7.Single stage LNA gain with composite MOS model

B. *S-parameter analysis*

The s-parameter extraction is done for the equivalent circuit model with the lumped elements constituting the extrinsic and intrinsic parts. This analysis is done in Ansoft Designer. The equivalent circuit parameter analysis is found to compare the different s-parameters showing the real and imaginary variables. The graphs shows different parameter extraction modeling results at high frequency. The S-parameter extraction is done for the two de-embedding techniques, that is with symmetric and non-symmetric de-embedding methods used and the noise figures are also verified for the same.

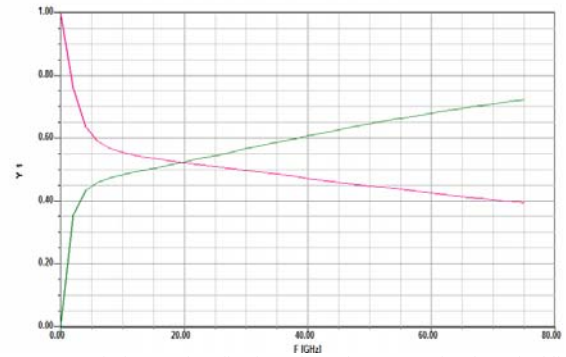

Fig8. Transmission and reflection through symmetric de-embedding network

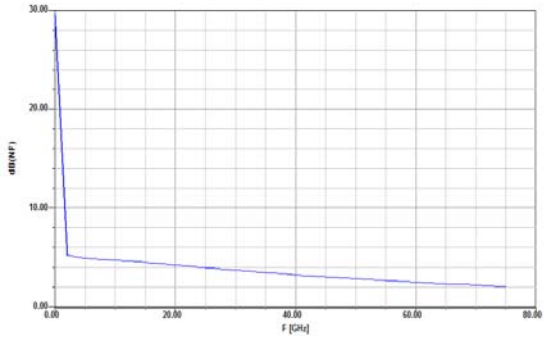

Fig.9. Noise figure NF=2.55 dB at 60GHz

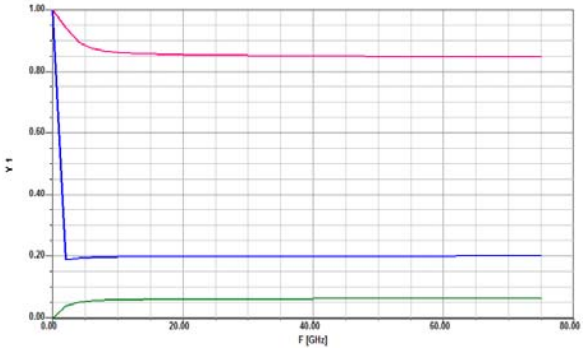

Fig.10. Transmission and reflection through non symmetric de-embeding network.

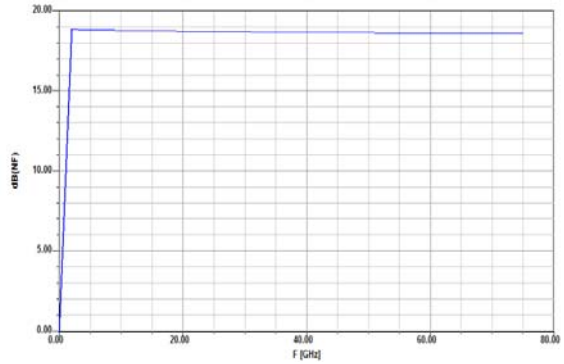

Fig.15. Noise figure NF=19dB AT 60GHz

VII. RESULTS AND DISCUSSION

The paper discusses on the designing and modeling of MMIC MOSFET. The modeling of both intrinsic and parasitic components in MOSFETs is crucial to describe the HF behaviour of CMOS devices operated at GHz frequencies. The brief discussion of the MOSFET modeling at millimetre wave frequency is done. Pads and interconnect lines are de-embedded, the parametric extraction calculations are done. The proposed scalable model is validated by comparing the measured and predicting parameters of the scaled devices up to 60 GHz.

VIII. CONCLUSION

The above work discusses on the designing and modeling of MMIC MOSFET. The modeling of both intrinsic and parasitic components in MOSFETs is crucial to describe the HF behaviour of CMOS devices operated at GHz frequencies. The brief discussion of the MOSFET modeling at millimetre wave frequency is done. The LNA design consisting of single stage is found to have better gain and with the inclusion of the designed composite MOS model it is found that the circuit gives better performance in the aspect of gain. Thus the above model is found to work at millimeter-wave frequency application. The s-parameter analysis also shows the efficient working of the model at high frequency.

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