On-Chip Optical Interconnects: A Viable Approach

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***Abstract*- Three decades ago Gordon Moore predicted that number of transistors per integrated circuit (IC) would double every two years. Today the high performance ICs are counting upto two billion of transistors and working at 10 GHz clock frequencies. The on chip interconnects are going to be a major bottleneck to the performance of such ICs. The use of copper interconnects & low K dielectrics has provided one time improvement of resistivity and electromigration, but with this the global interconnect performance required for future generations of ICs cannot be achieved. In this paper, optical interconnects which is the most promising approach to interconnect problem has been discussed. Also the performance of opical interconnects and copper interconnects for intrachip global signaling is compared.**

***Keywords*- Electrical interconnects, optical interconnects, global interconnects, 3D and RF interconnects.**

I. INTRODUCTION

As shown by ITRS [1] the metal layer pitch and transistor gate length has been decreasing and over the years in future technologies also it is going to follow the same pattern as shown in Fig 1. The miniaturization of interconnects unlike transistors doesn't enhance their performance. Scaling interconnects not only degrades the delay but it also effects other non-ideal factors like material integration, electrical, mechanical and thermal stress in metal layers etc. Also small feature sizes and high clock periods result in high switching activity in capacitive and inductive coupling. The reduced supply voltage levels make the wires more susceptible to noise. Most importantly the power consumption is increased with increase in switching activities of capacitive wire. Using the shielding techniques and by increasing the wire spacing the problem of delay and noise may be solved up to a good extent but it leads to inefficient use of interconnect resources.

A potential solution to these interconnect problem is the use of an optical interconnect layer. The properties of optics like high bandwidth, electromagnetic noise immune, very less temperature variations, time predictability or synchronous operation can empower the interconnects in coming technologies.

II. ELECTRICAL INTERCONNECTS

A. *Resistance*

The most important thing to observe in metallic interconnect is that they cannot scale with transistor size.

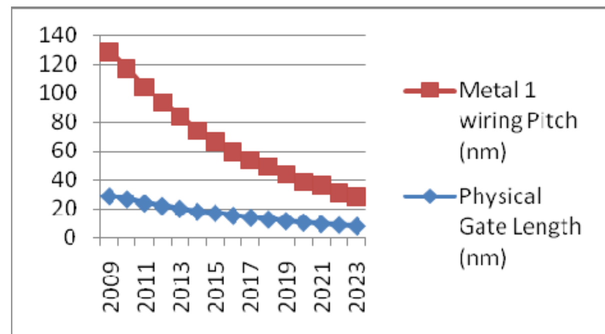

Fig 1 Trend for the physical gate length and metal 1 wiring pitch

Scaling reduces the dimensions h and w (height and width respectively Fig 2). Therefore, resistance of the wire per unit length is given by

$$R = \frac{\rho}{(h)(w)} \qquad (1)$$

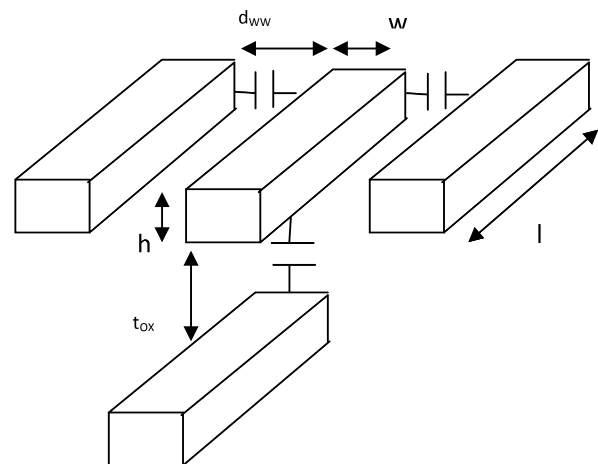

Fig 2 Crossectional view of a metal conductor

The cross-sectional area is reduced by s^2 where s is the scaling factor. Thus the resistance R is increased by $1/s^2$. This increase in resistance can be avoided by using inverse scaling strategy. In this the 'w' is decreased by s whereas 'h' is increased by the same factor to keep cross-sectional area

constant. However, this increases the sidewall capacitance. Also the height of the metal layers cannot be increased indefinitely to maintain planar geometry. So ultimately resistivity is the only variable that can decrease the resistance per unit length. Then came the copper wires which have smaller value of resistivity (2.2 µcm) as compared to aluminum wires (3.34 µcm). The use of copper brought a major breakthrough but now it has also reached its limit. Also in the future technologies skin effect for most on chip wires will not be negligible.

B. Capacitance

For a given w the capacitance can be modeled as [2]

$$C_{wire} = \varepsilon_0 \left(2K\varepsilon_h \frac{h}{d_{ww}} + 2\varepsilon_v \frac{w}{t_{ox}} \right) + fringe(\varepsilon_h, \varepsilon_v) \quad (2)$$

Where ε_h,ε_v, and ε_0 are the horizontal relative, vertical relative and absolute dielectric constants. This equation shows that capacitance can be decreased either by reducing h or w and by increasing d_{ww} or t_{ox}. 'h' and 'w' cannot be decreased much as it will increase resistance whereas d_{ww} (wire to wire spacing) also cannot be increased in current technology. So ε_h,ε_v are the only variables left to control the capacitance of wires. This has been implemented using low k dielectrics but such materials are susceptible to thermal and mechanical stress.

C. Delay

The RC delay varies with l_w^2 [3] where l_w is the length of wire from an emitter gate to receiver gate through which we want to measure the propagation delay. This quadratic dependence can be made linear by inserting repeaters but that eventually leads to more power and area consumption.

The delay of local wires that scale in length don't worsen much with technology whereas delay for global wires that do not scale in length doubles with each technology [2]. So looking at the performance of electrical interconnects it is obvious that the change in materials or improving the criterion of design is no longer going to satisfy the performance requirements of the future technologies. We need to have an interconnect innovation i.e. altogether a new technology to meet or fulfill those requirements.

III. OPTICAL INTERCONNECTS

A promising approach to interconnect problem is the use of optical interconnect layer. This approach has been the subject of research for at least 25 years. It started with the paper of Goodman et. al [4]. Since then many researchers have discussed the potential benefits and limits of optical interconnections [5]-[8]. Some papers have also discussed the hybrid technologies of fabricating optical components [9], [10].

An optical interconnect system (Fig. 3) consists of an off-chip laser, an optical modulator, a polymer waveguide and an optical detector. Such an optical system can be implemented

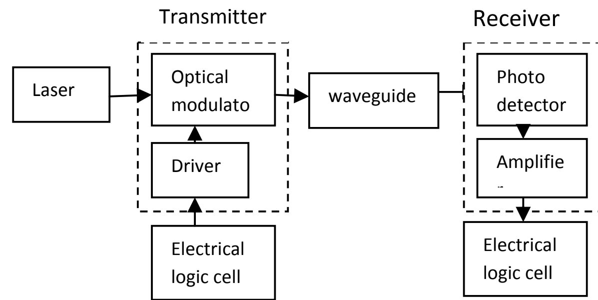

Fig 3 On Chip Optical Interconnect System

and performs better at the places where there is need to broadcast a signal to many nodes for example clock distribution or may be DRAMs (Fig. 4).

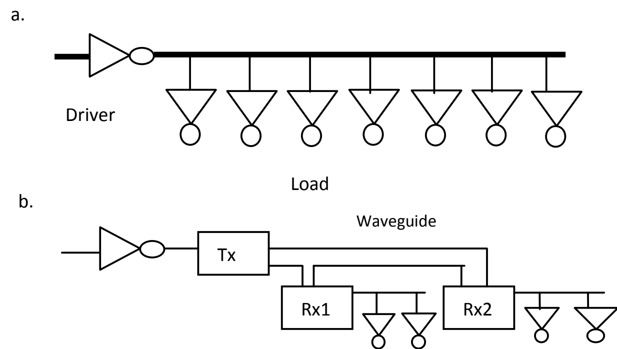

Fig 4 a) Schematic of an electrical driver driving a large load.
b) Schematic of an alternative optical system

By using electrical fanout architecture as shown in Fig 4a) the capacitive loads of fanout will degrade delay and bandwidth badly. The Fig 4b) using an optical fanout architecture will provide a better solution which can solve the problem of low bandwidth of electrical wires and high latencies of electrical fanout systems [8]. Whereas for an optical fanout of one the delay in such system would be worse than the delay in electrical systems. But there lies a critical length beyond which the optical interconnects become faster than the fastest copper interconnects [7]. Also for chip edge long interconnects optical interconnects have very small delay value with comparable power expenditure. Also with switching activity for long links optical interconnect always offer lower delay and lower power dissipation.

Optical interconnects being one of the most viable approach there are other alternative interconnect technologies available like Integrated Radio frequency and Microwave Interconnects [11] and 3D integration [12].

A. Alternative Interconnect Technologies

1)Radio Frequency Interconnect: RF signals at chip level can be transmitted through waveguide. A wireless LAN type architecture Fig 5 uses high bandwidth i.e. upto 200 GHz. The encoding techniques like CDMA (Code Division Multiple

Access) or FDMA (Frequency Division Multiple Access) may be used. This approach is good for parallel computing and can offer an attractive solution to reconfigurable and fault tolerant architectures. But this technology shows incompatibility with CMOS in terms of circuit operating frequency (GHz) with maximum carrier frequency (100GHz), high silicon area and power consumption.

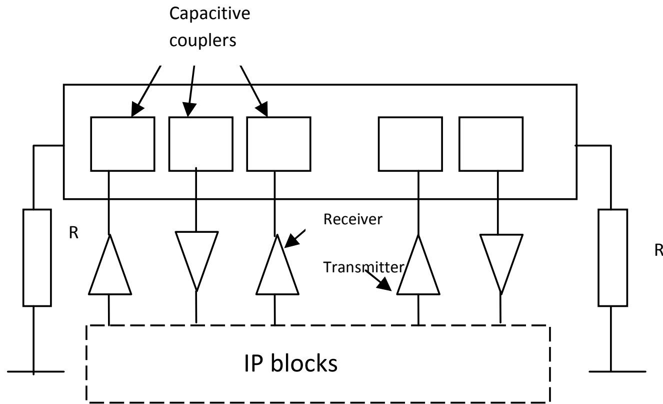

Fig 5 RF Interconnect channel

2) 3D Integration: This technology offers multilayered architecture as shown in Fig. 6 There are vertically stacked

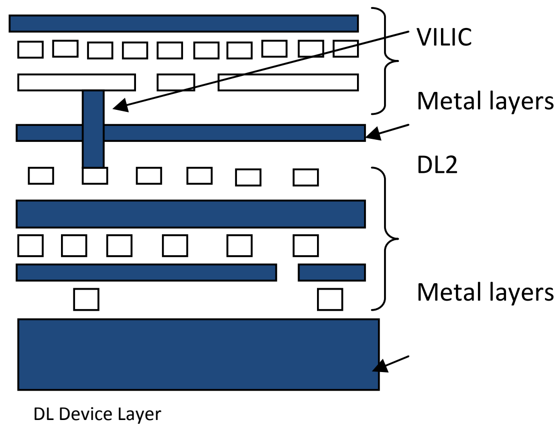

Fig 6 Schematic representation of 3D integration

layers of different blocks of an IC. Each layer has several layers of interconnections and interlayer vias between the layers. This technology provides more flexible architectural designs, placement and routing. More interestingly there are no global interconnects. They are replaced by short interlayer vias to route vertically. However, problems like thermal evacuation and high reliability of components, crosstalk in upper metal layers are major technical barriers to the use of this technology.

Among all these alternative technologies the optical interconnects show better possibilities of being used which can be seen from Table 1. So now some of the advantages and technical challenges for optical interconnects can be enlisted.

TABLE1
COMPARISON OF ALTERNATIVE INTERCONNECT APPROACHES

	RF interconnect	**3D interconnect**	**Optical interconnect**
Bandwidth	High	Better than 2D	High
Delay	Limited by medium	Good	Limited by devices
Density	High	High	High
Power consumed	High	Low	Low
Voltage isolation or crosstalk	Poor	Good	Good
Physical safety	Bad	Bad	Good
Modifications required	No	Yes	Yes

B. *Advantages*

1) High speed: Carrier frequency of optics is very high which allows no degradation in signal propagation with increase in frequency of modulation.

2) Deterministic timing behavior: The fact is that light propagates in optical fiber slowly as compared to coaxial cable because of the refractive index of glass and velocity of light gives rise to delay but the optical signal arrival is reliable and predictable which can be applied to systems such as clock distribution.

3) Increased interconnect density: Use of wavelength division multiplexing (WDM) technique can increase the data rate of optical link.

4) Low power and Area: In optics power consumption doesn't depend on the distance of signal propagation. So optics can be used to eliminate the high power clock drive circuits on chip which are power and area hungry.

5) Signal Isolation: The difficulties like impedance matching, wave reflection and crosstalk can be avoided in optics which become prominent in electrical interconnects.

TABLE 2
COMPARISON BETWEEN ELECTRICAL AND OPTICAL INTERCONNECTS

	Electrical interconnect	**Optical interconnect**
1.	Delay depends on temperature	Delay doesn't depend on temperature
2.	Clock drive circuits for synchronization	Predictability of time eliminates such circuits
3.	Reflection from capacitive loads	Optical signal not reflected from electrical capacitances
4.	Finite inductances generate voltage	No analogous phenomenon in optics
5.	Detects RF signal	Doesn't detect RF signals
6.	Increased clock speeds need redesigning	Redesigning not required with clock speed increase.

C. Technical Challenges:

There are some important technical challenges for optical interconnects which has to be faced and solved before taking this technique forward for implementation. These have been discussed in detail by some authors [5], [6], [13], [14] however few of them are being discussed here:-

1) *Receiver circuits:* Majority of the power in an optical system is consumed by the receiver circuit. So its integration is very important for a good performance. Also to keep their power dissipation and area small the input capacitance essentially have to be small.

2) *Optoelectronic devices:* The devices like quantum well modulators, VSCELs, LEDs and waveguides require evolutionary improvements to be compatible with low voltage future generations of silicon ICs [5], [6], [8].

3)*Appropriate practical Opto-mechanical technology:* The most serious issue in implementation of optical interconnects is the absence of low cost practical optomechanical technology. However, a viable approach is the use of hybrid integration technique like solder bonding has been reviewed [15], [16]. This requires continued research for making integration of dense optical interconnects to chip practical.

IV. CONCLUSION

This is quite clear that the problems of metal interconnects cannot be totally eliminated by electrical solutions. No doubt such solutions can stretch the performance of electrical interconnects for some time but there is need to have a physical solution and optical interconnects have emerged as the best option. The advantage of using optical interconnects for global wires or clock distribution are well understood (Table 2). This can solve the underlying problems like voltage isolation, wave reflection, impedance matching, system synchronization, power dissipation in clock drive circuits and global interconnects of electrical wires and also has potential to cope up with the future generations of ICs. However major technical issues like their compatibility and fabrication with silicon are to be sorted out.

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